K72JK Schematic R2.0

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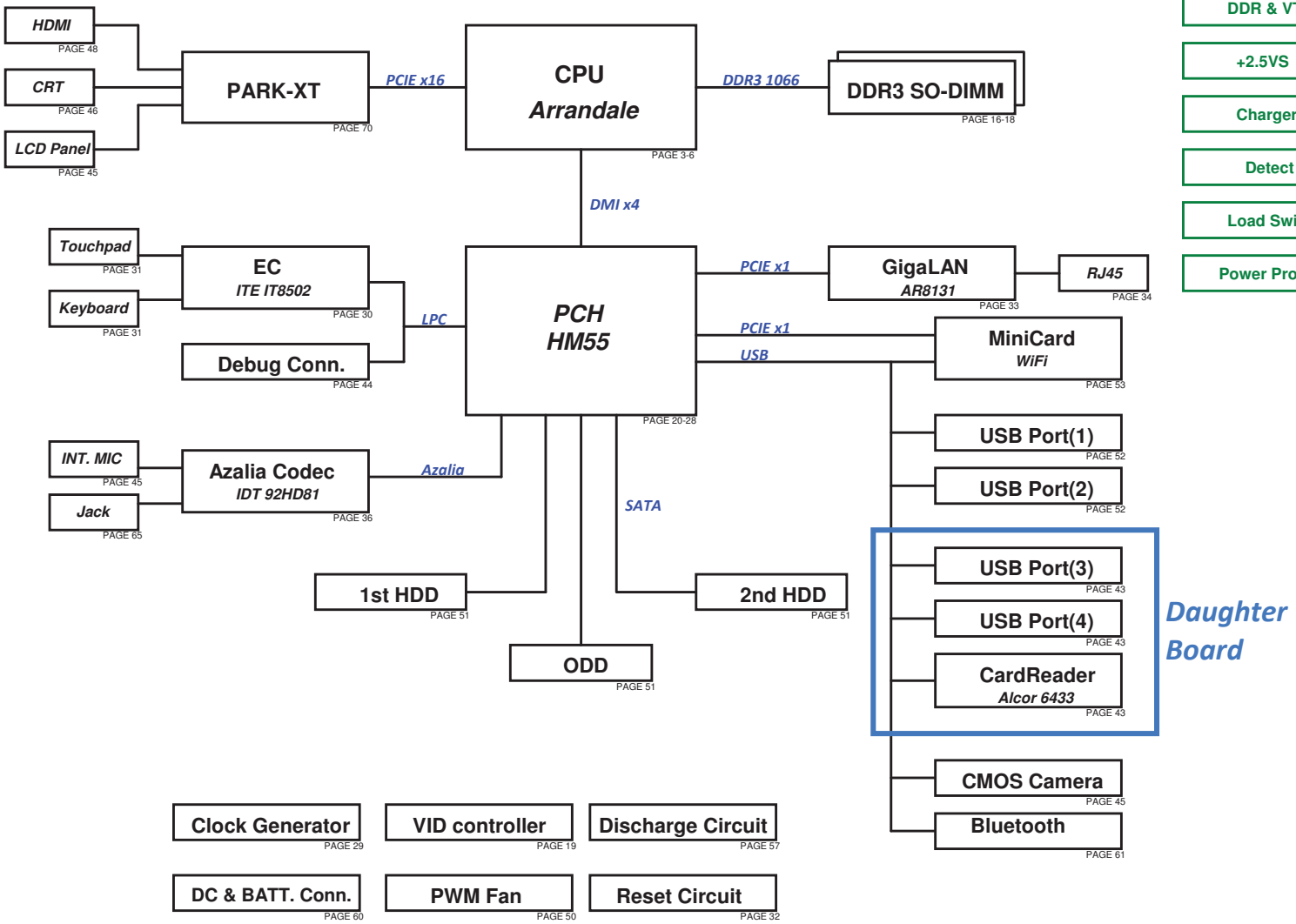

Power

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ASUSTeK COMPUTER INC. NB4	Title : Block Diagram	
	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, January 22, 2010	Sheet 1 of 99	

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EC IT8512

PCH GPIO	Usage	Signal Name	Pull Up / Pull Down	Power
GPIO 00	GPO			+3VS
GPIO 01	GPO		INT PU 20K	+3VS
GPIO [02:05]	Native	PCI_INT[E:H]#	EXT PU 10K	+5VS
GPIO 06	GPO		INT PU 20K	+3VS
GPIO 07	GPO		INT PU 20K	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC#5	EXT PU 10K	+3VSUS
GPIO 10	Native	USB_OC#6	EXT PU 10K	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU 10K	+3VSUS
GPIO 12	GPO			+3VSUS
GPIO 13	GPO		INT PD 20K	+3VSUS
GPIO 14	GPO	USB_OC#7	EXT PU 10K	+3VSUS
GPIO 15	GPO	BT_LED	INT PD 20K	+3VSUS
GPIO 16	GPO		EXT PU 10K	+3VS
GPIO 17	GPO		INT PU 20K	+3VS
GPIO 18	Native	CLKREQ1#	EXT PU 10K	+3VS
GPIO 19	Native	SATA1GP	EXT PU 10K	+3VS
GPIO 20	Native	CLKREQ2#	EXT PD 10K	+3VS
GPIO 21	Native	SATA0GP	EXT PU 10K	+3VS
GPIO 22	GPO	WLAN_LED		+3VS
GPIO 23	GPO		INT PU 20K	+3VS
GPIO 24	GPO			+3VSUS
GPIO 25	Native	CLKREQ3#	EXT PU 10K	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU 10K	+3VSUS
GPIO 27	GPO		INT PU 20K	+3VSUS
GPIO 28	GPO	WLAN_ON#	INT PU 20K	+3VSUS
GPIO 29	GPO			+3VSUS
GPIO 30	Native	ME_SusPwrDnAck	EXT PU 10K	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU 10K	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU 10K	+3VS
GPIO 33	GPI	PCH_SPI_OV	INT PU 20K	+3VS
GPIO 34	Native	STP_PCI#		+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PD 10K	+3VS
GPIO 36	GPO		EXT PU 10K	+3VS
GPIO 37	GPO		EXT PU 10K	+3VS
GPIO 38	GPI	PCB_ID0	EXT PU/PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PU/PD	+3VS
GPIO 40	Native	USB_OC#1	EXT PU 10K	+3VSUS
GPIO 41	Native	USB_OC#2	EXT PU 10K	+3VSUS
GPIO 42	Native	USB_OC#3	EXT PU 10K	+3VSUS
GPIO 43	Native	USB_OC#4	EXT PU 10K	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU 10K	+3VSUS
GPIO 45	Native	CLK_REQ6#	INT & EXT PU	+3VSUS
GPIO 46	GPO			+3VSUS
GPIO 47	Native	CLKREQ_PEG#A	EXT PD 10K	+3VSUS
GPIO 48	GPO			+3VS
GPIO 49	Native	TEMP_ALERT#	EXT PU 10K	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU 10K	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU 20K	+3VS
GPIO 52	Native	PCI_REQ2#	EXT PU 10K	+5VS
GPIO 53	Native	PCI_GNT2#	INT PU 20K	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PU 10K	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU 20K	+3VS
GPIO 56	Native	CLKREQ_PEG#B	EXT PU 10K	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU 10K	+3VSUS
GPIO 59	Native	USB_OC#0	EXT PU 10K	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU 10K	+3VSUS
GPIO 61	Native	SUS_STAT#		+3VSUS
GPIO 62	Native	SUSCLK		+3VSUS
GPIO 63	Native	SLP_S5#		+3VSUS
GPIO 64	Native	CLK_OUT0	INT PD 20K	+3VS
GPIO 65	Native	CLK_OUT1	INT PD 20K	+3VS
GPIO 66	Native	CLK_OUT2	INT PD 20K	+3VS
GPIO 67	Native	CLK_CARD_READER_48	INT PD 20K	+3VS
GPIO 72	Native	PM_BATLOW#	INT PU 20K	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU 10K	+3VSUS
GPIO 74	Native	SML1ALERT#	EXT PU 10K	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU 10K	+3VSUS

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2		CHG_FULL_LED#
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6		-
GPA7		-
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2		ME_AC_PRESENT_EC
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0		-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	-
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		SD_CD#_EC
GPE0	O	VSUS_ON
GPE1	O	-
GPE2	O	-
GPE3	O	-
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7		-
GPF0	O	-
GPF1		-
GPF2	I	-
GPF3		-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7		PCH_SPI_OV
GPG0		ME_SusPwrDnAck_EC
GPG1	I	PM_SUSB#
GPG2	O	OCMV_CTL0
GPG6	O	OCMV_CTL1
GPH0	IO	PM_CLKRUN#
GPH1	O	-
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0		-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5	I	-
GPI6	I	-
GPI7	I	-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	-
GPJ5		-

EC GPIO	Use As	Signal Name
GPIO0	I	
GPIO1	I	
GPIO2		-
GPIO3		-
GPIO4	I	
GPIO5	I	
GPIO6	O	
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		-
GPIO11		-
GPIO12	O	
GPIO13		-
GPIO14	O	
GPIO15		-
GPIO16		-
GPIO17		-
GPIO18		-
GPIO19		-
GPIO20		-
GPIO21		-
GPIO22		-
GPIO23		-
GPIO24		-
GPIO25		-
GPIO26		-
GPIO27		-
GPIO28		-
GPIO29		-
GPIO30		-
GPIO31		-
GPIO32		-
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		-
GPIO37		-

PCIE 1	
PCIE 2	Minicard WLAN
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	

	K72J
0	USB port
1	USB port
2	USB port (D/B)
3	USB port (D/B)
4	
5	MiniCard (Full)
6	
7	
8	MiniCard (Half)
9	Camera
10	
11	Card Reader
12	Bluetooth
13	

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LRS3162)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
CPU Thermal Sensor(G781)	1001100x (98)	
VGA Thermal IC(G781-1)	1001101x (9A)	

Device Identification

	CPU Thermal Sensor P/N:	component name
1st	06G023048011	G781F
S		
S		
S		

	Clock Gen P/N:	component name
1st	06G011610010	ICS9LRS3162
S		
S		

	VGA Thermal Sensor	component name
1st	06G023048020	G781-1
S		
S		

ASUSTeK COMPUTER INC. NB4

Title : System Setting

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	K72Jr	2.0

Date: Friday, December 11, 2009 Sheet 2 of 99

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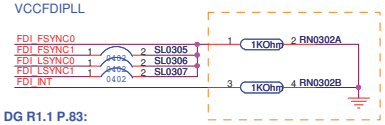
FDI disable: (For discrete graphic)

1. NC:
   FDI_TX#[0:7],FDI_TX[0:7],FDI_RX#[0:7],FDI_RX[0:7]
   VCC_AXGSENSE,VSS_AXGSENSE
2. Pull-down to GND via 1KΩ ± 5% resistor:
   FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON
   ~15mW power saving.(DG R0.8 P.70)
3. Connected to GND:
   VCCAXG,
4. Can be connected to GND directly:
   DPLL_REF_CLK,DPLL_REF_CLK#
5. Connect to +V1.05S rail:
   VCCFDIPLL

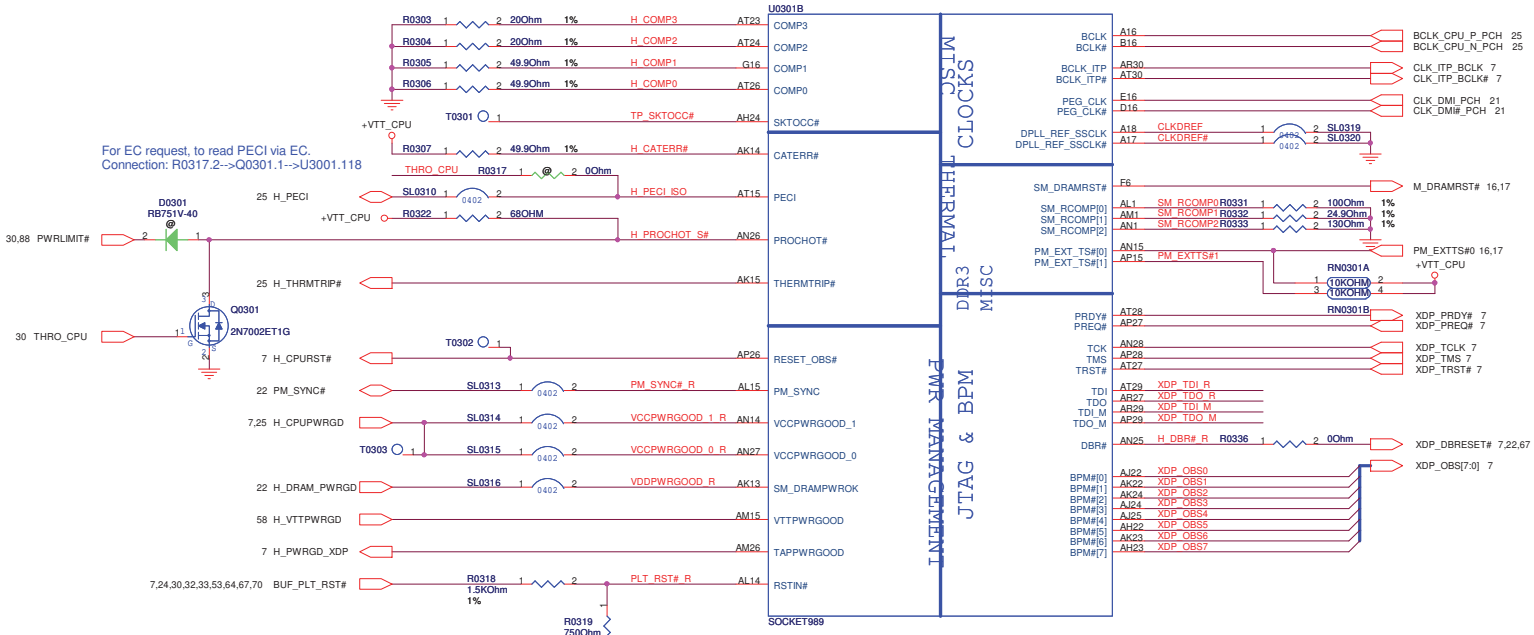


DG R1.1 P.83:

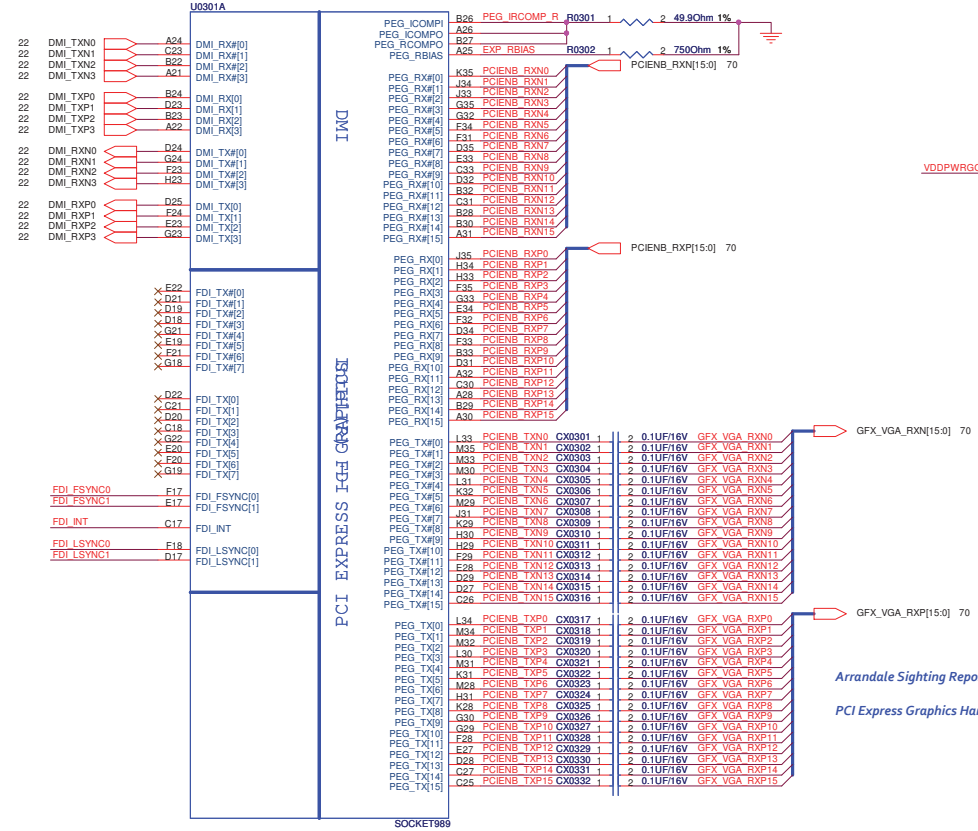
*FDI_FSYNC[0],FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor.
*On the other hand,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

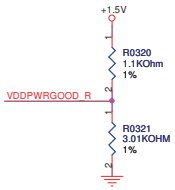
Arrandale Sighting Report :

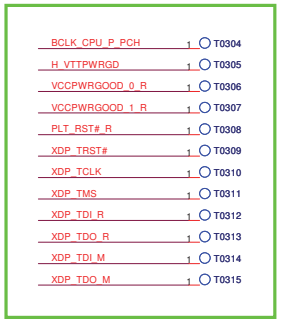
System May Hang With DMI L1 Enabled.



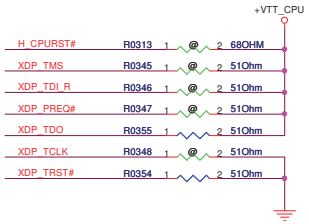
CPU Socket : 12G011909890
Molex : 12G011909891
Tape & Reel : 12G011909893



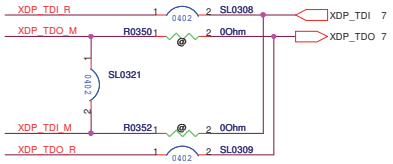




For CPU Boundary Scan



JTAG MAPPING



Arrandale Sighting Report :

PCI Express Graphics Hang With L1 Enabled in Rare Cases.

DG R1.1 P.109:

*On Clarksfield rPGA only designs, VCCPWRGOOD_1 on the Clarksfield processor can be left as No Connect.

ASUS	Title : CPU(1)_DMI,PEG		
ASUSTeK COMPUTER INC. NB1	Engineer: Jerry Mou		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, December 11, 2009	Sheet 3 of 99		

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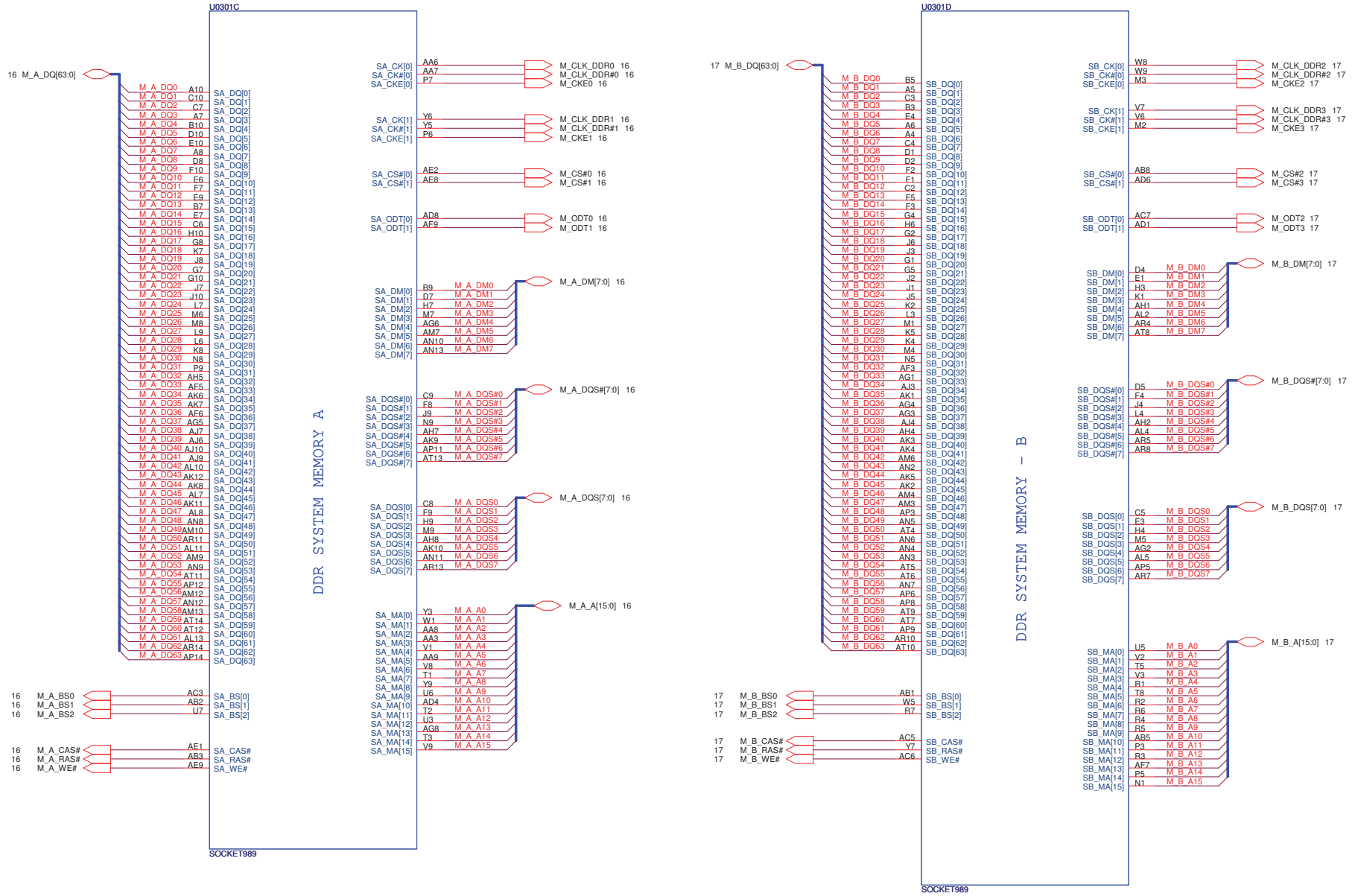

ASUSTeK COMPUTER INC. NB1

Title : CPU(2)_DDR3

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	K72Jr	2.0

Date: Friday, December 11, 2009 Sheet 4 of 99

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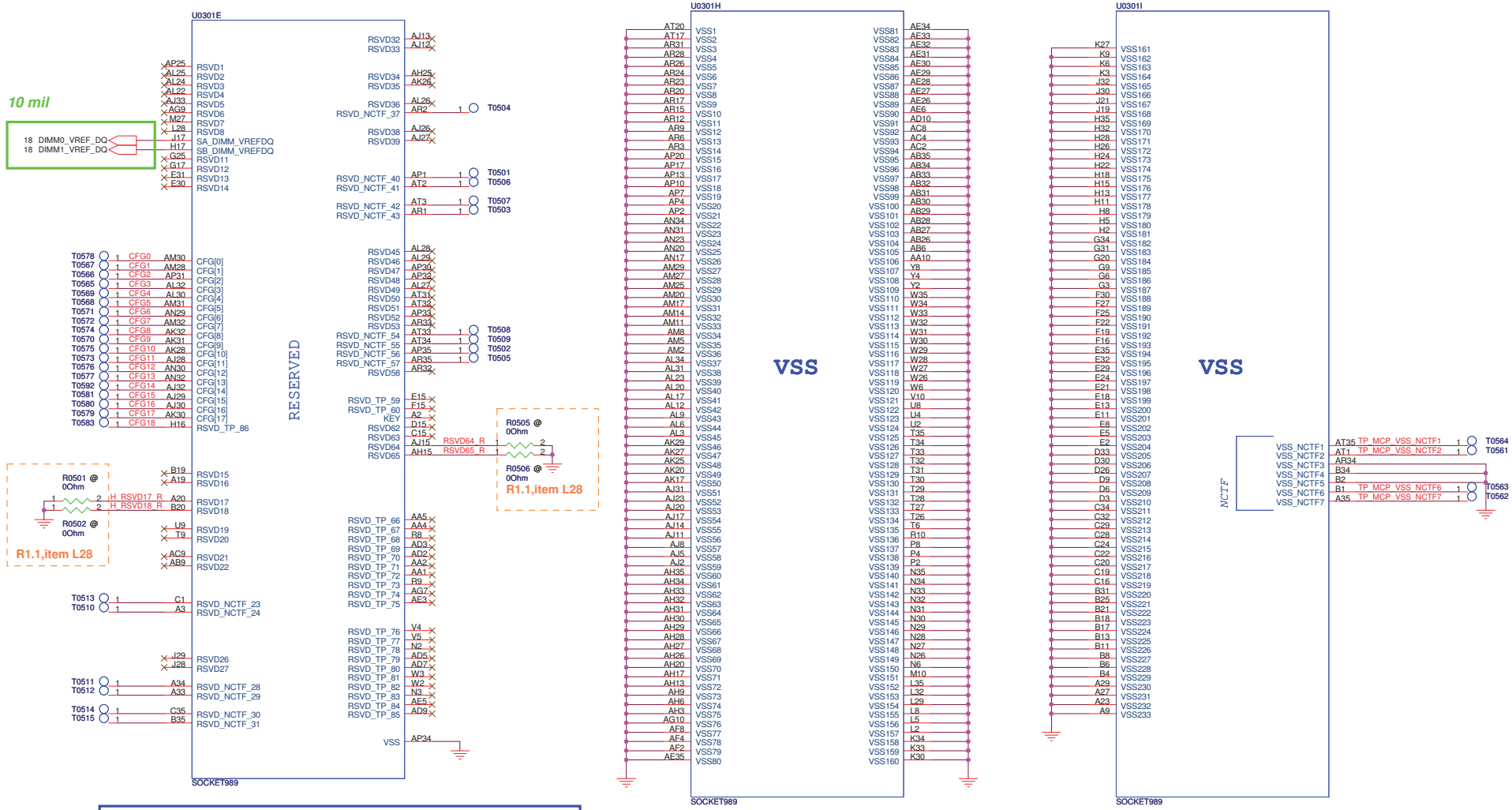

CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIE Static Numbering Lane Reversal.(Auburndale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)

Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor

For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.

Intel sighting #: 402607(3393727)

To drive a value of zero on CFG[0] pin use a 250 Ohm pull down resistor to Vss.

CFG0 R0535 1 @ 2 3.01KOHM 1%

CFG4 R0537 1 @ 2 3.01KOHM 1% eDP=3.3K PD

CFG3 R0536 1 @ 2 3.01KOHM 1%

CFG7 R0538 1 @ 2 3.01KOHM 1%

Unmount R0501& R0502 & R0505 & R0506 for Intel CRB sugesstion.

ASUSTeK COMPUTER INC. NB1	Title : CPU(3)_CFG,GND	
	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
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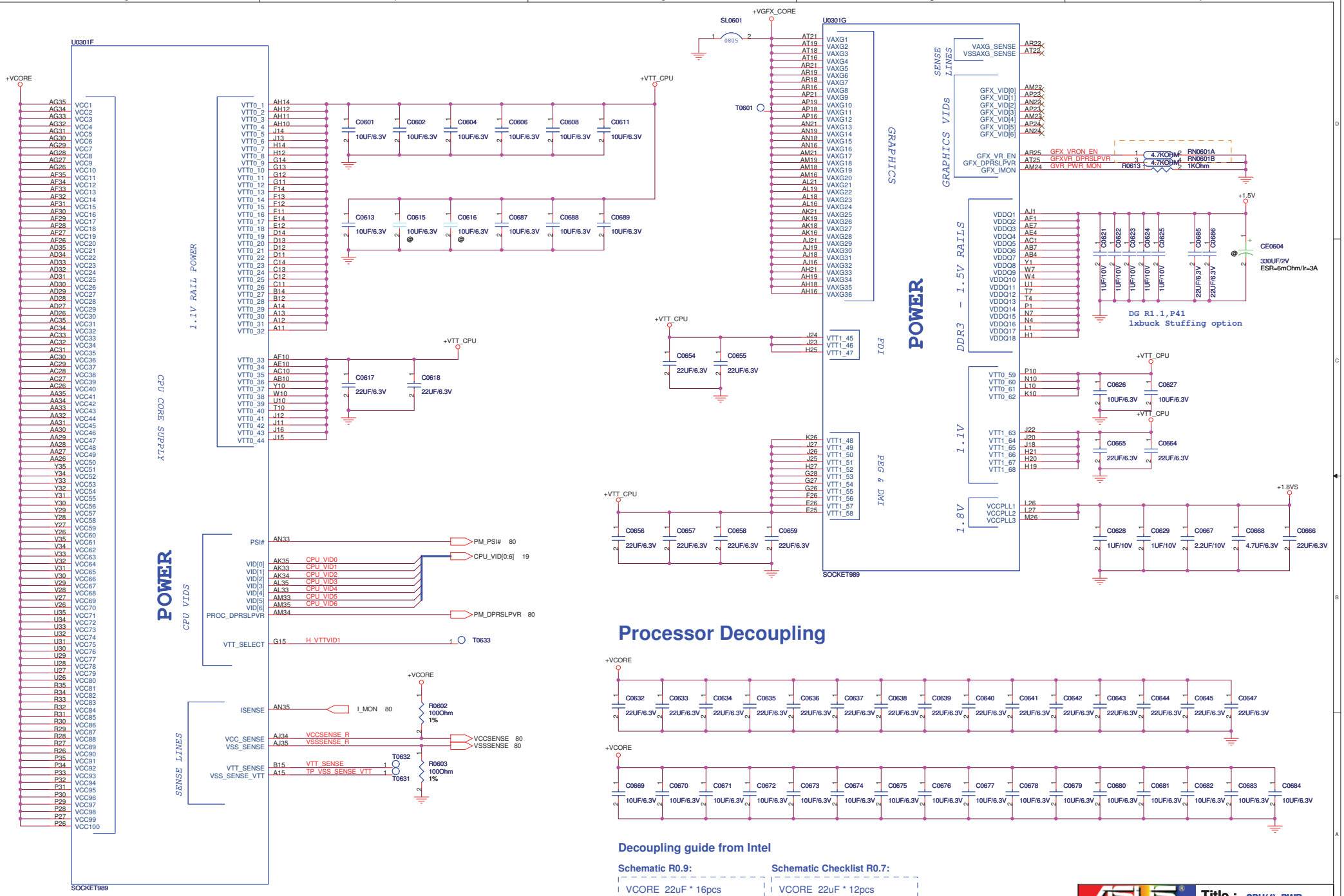

Processor Decoupling

Decoupling guide from Intel

Schematic R0.9:	Schematic Checklist R0.7:
VCORE 22uF * 16pcs	VCORE 22uF * 12pcs
10uF * 16pcs	10uF * 16pcs
470uF* 6pcs(2 no stuff).	470uF* 6pcs(2 no stuff).

ASUSTeK COMPUTER INC. NB1	Title : CPU(4)_PWR	Engineer: Jerry Mou
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 6 of 99	

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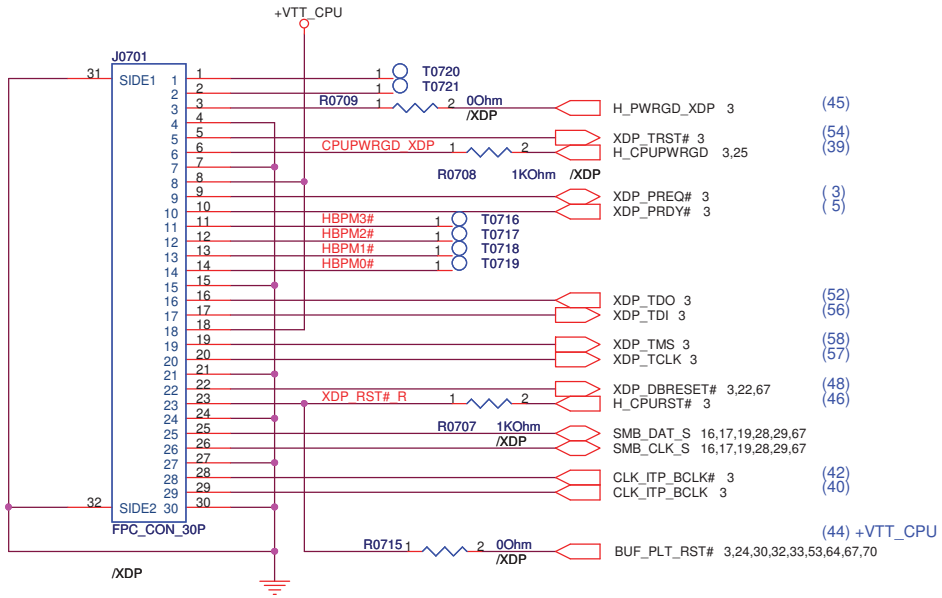
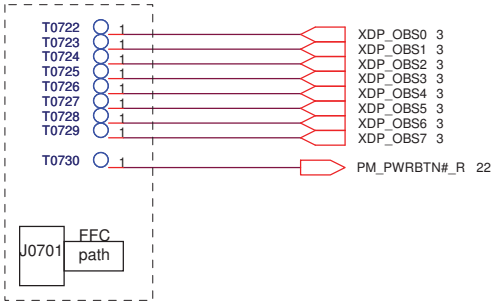
CPU XDP connector





Put these test point near J0701.

Put it away from the FFC path.

ASUS	Title : CPU(5)_XDP		
ASUSTeK COMPUTER INC. NB1	Engineer: Jerry Mou		
Size Custom	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009	Sheet 7 of 99		

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ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: K72Jr		Rev: 1.0
Date: Friday, December 11, 2009	Sheet 8 of 99		

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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 9 of 99	

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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 10 of 99	

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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 11 of 99	

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ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: K72Jr	Rev: 1.0
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: K72Jr	Rev: 1.0
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ASUSTeK COMPUTER INC. NB6	Title :	Engineer: Ryan_Wang
Size: A	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 14 of 99	

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ASUSTeK COMPUTER INC. NB6	Title :	Engineer: Ryan_Wang
Size: A	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 15 of 99	

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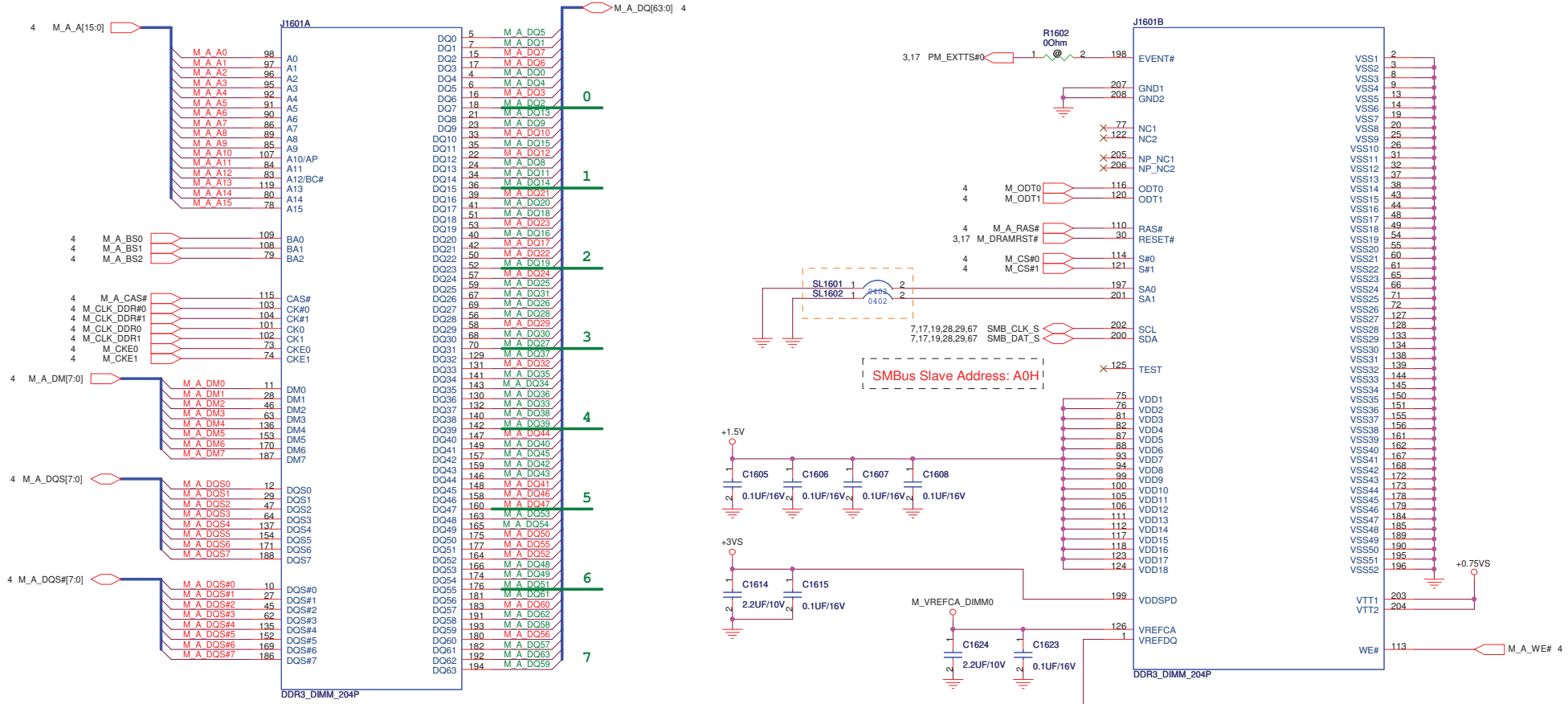
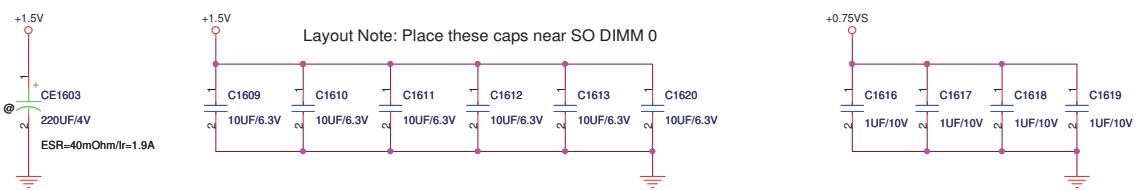


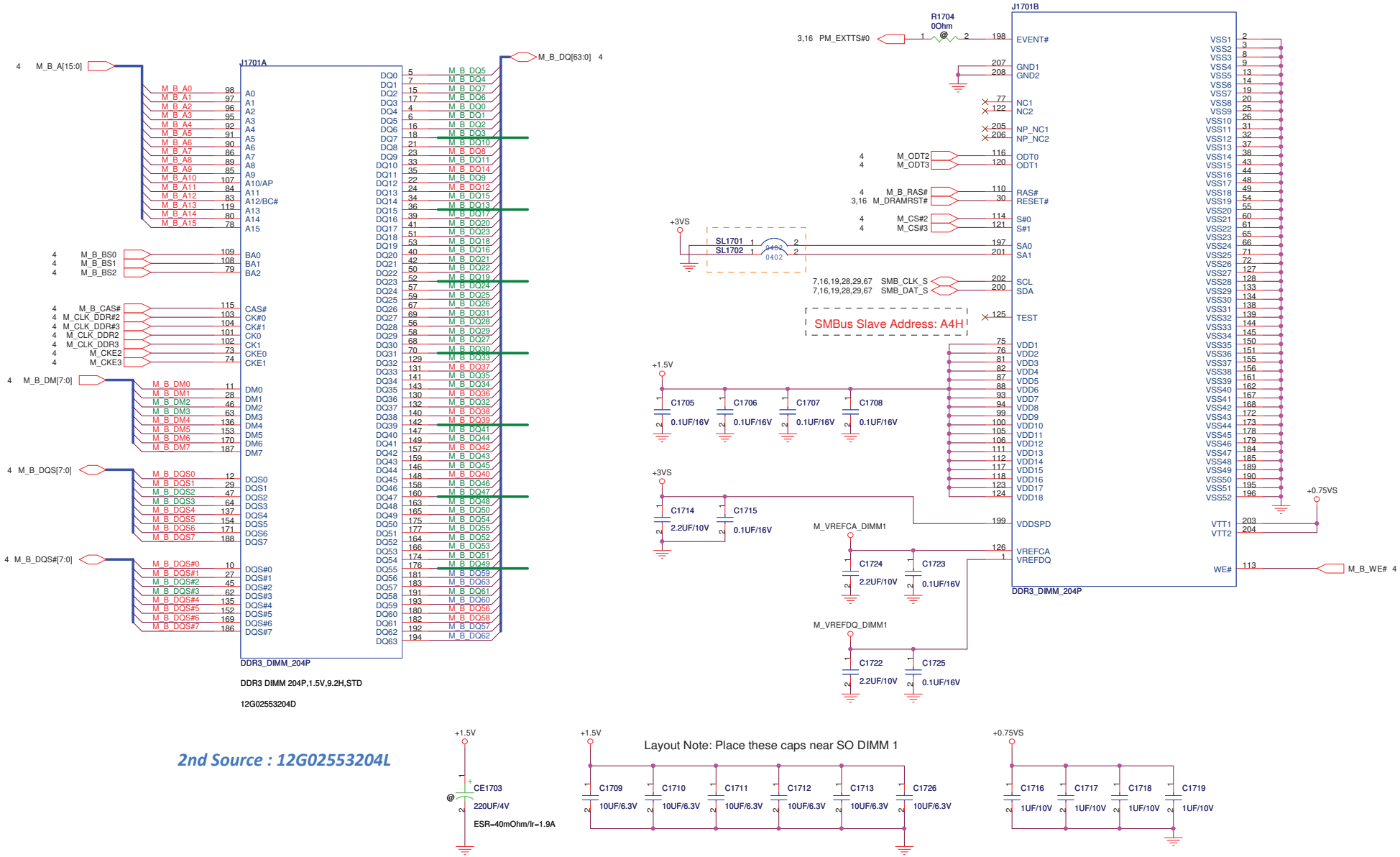
Tyco new P/N : 12G02553204G

2nd Source : 12G02553204K



ASUSTeK COMPUTER INC. NB6	Title : DDR3 SO-DIMM 0		
	Engineer: Jerry Mou		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, January 29, 2010	Sheet 16 of 99		

http://laptop-motherboard-schematic.blogspot.com/



2nd Source : 12G02553204L

ASUSTeK COMPUTER INC. NB6

Title DDR3 SO-DIMM_1

Engineer: Jerry Mou

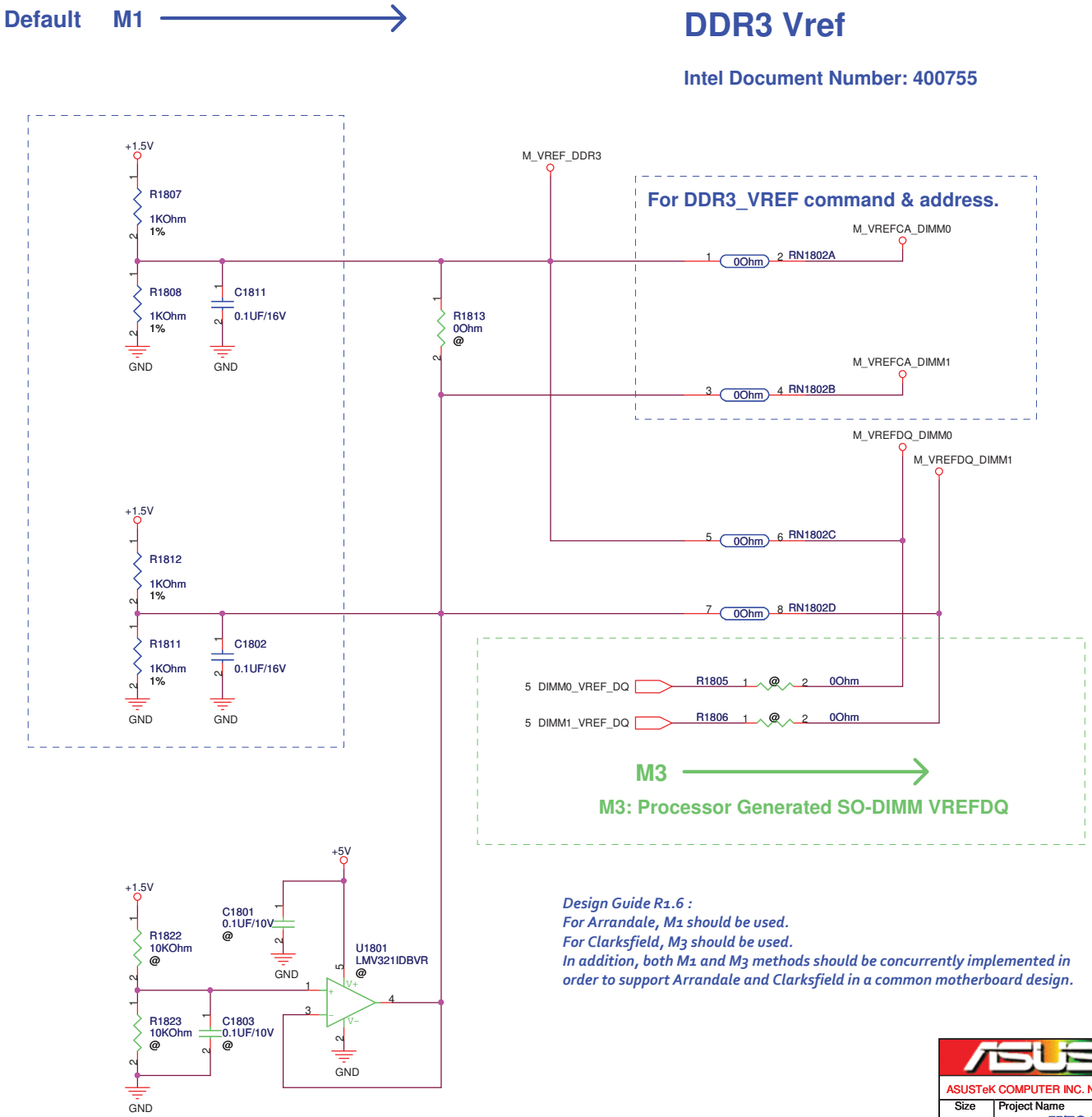
Size	Project Name	Rev
Custom	K72Jr	2.0

Date: Friday, January 22, 2010 Sheet 17 of 99

http://laptop-motherboard-schematic.blogspot.com/

DDR3 Vref

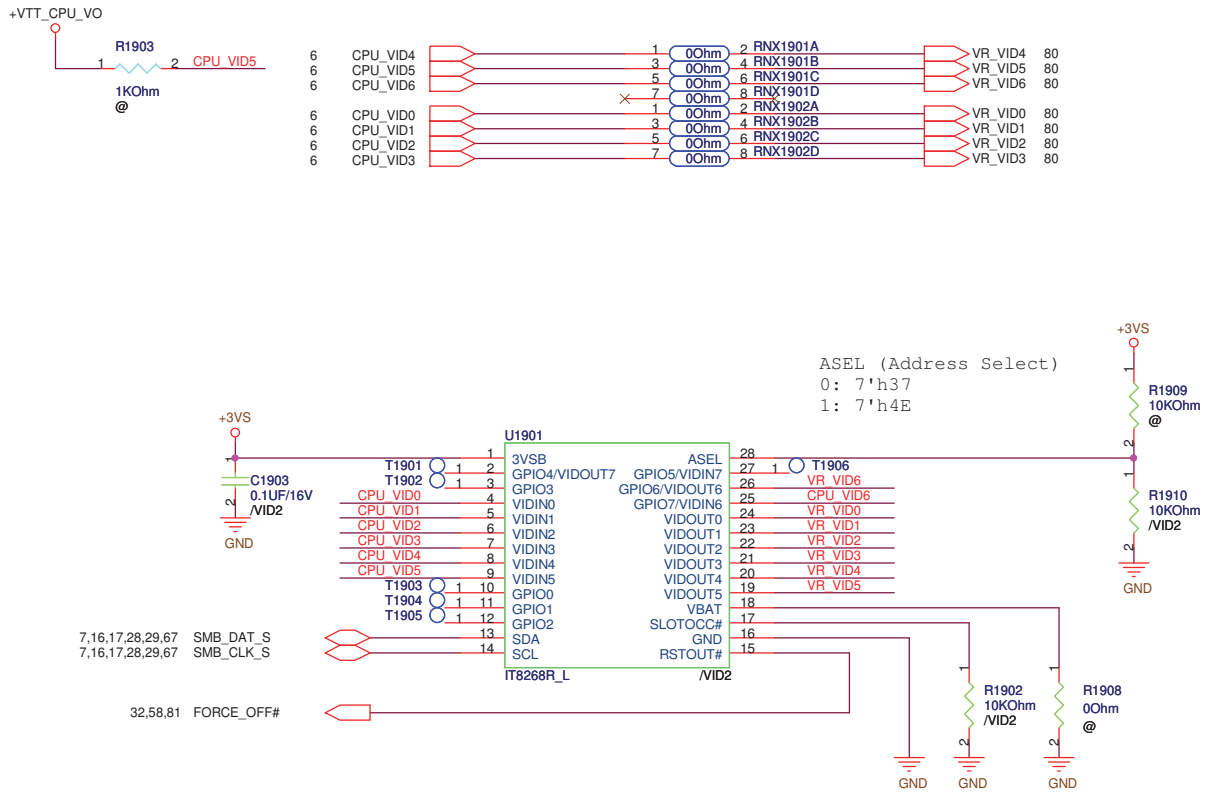
Intel Document Number: 400755



Design Guide R1.6 :
For Arrandale, M1 should be used.
For Clarksfield, M3 should be used.
In addition, both M1 and M3 methods should be concurrently implemented in order to support Arrandale and Clarksfield in a common motherboard design.

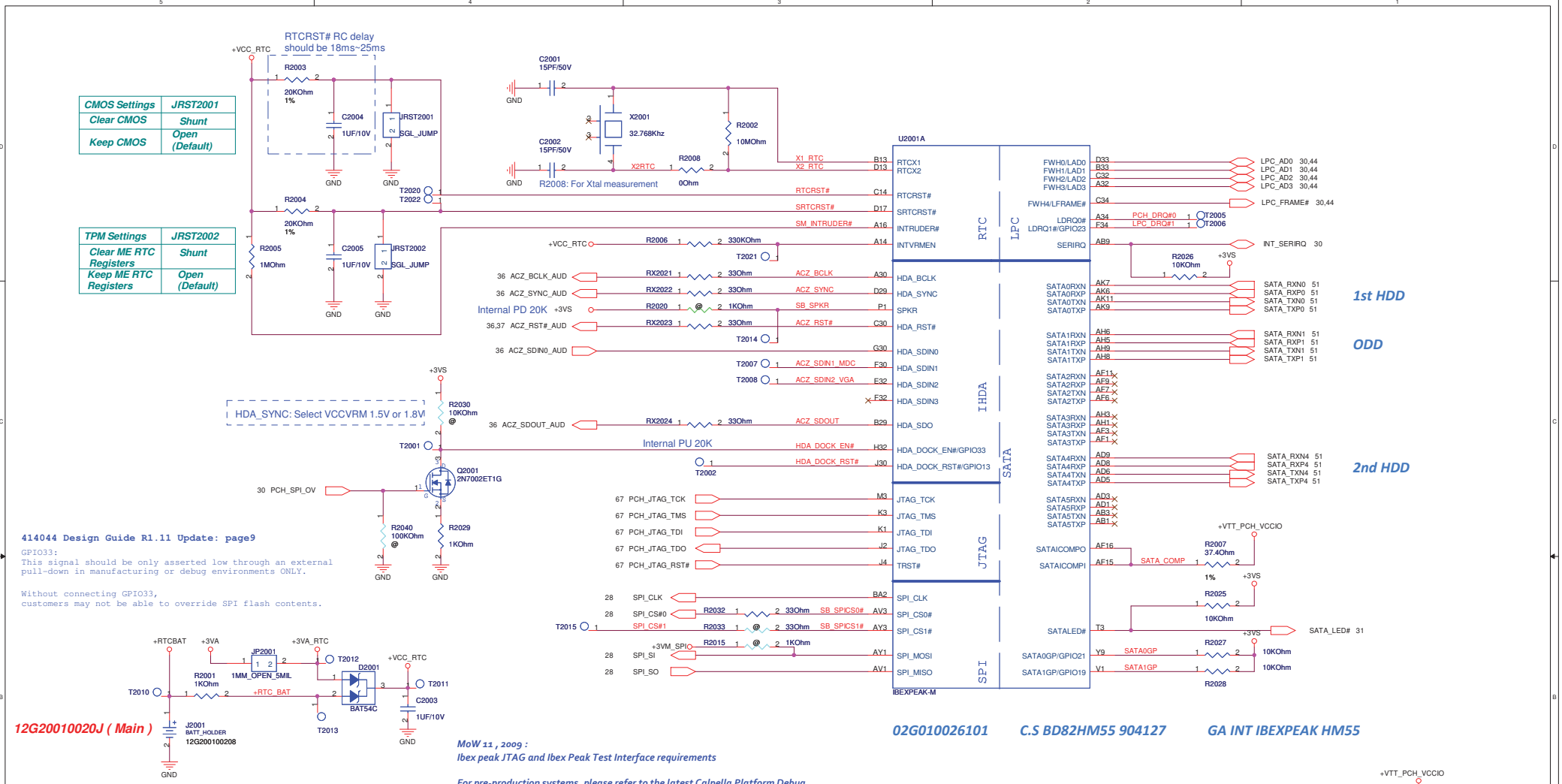
ASUSTeK COMPUTER INC. NB1	Title : DDR3 VREF	
	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 18 of 96	

http://laptop-motherboard-schematic.blogspot.com/



ASUS	Title : VID	
ASUSTeK COMPUTER INC. NB1	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 19 of 99	

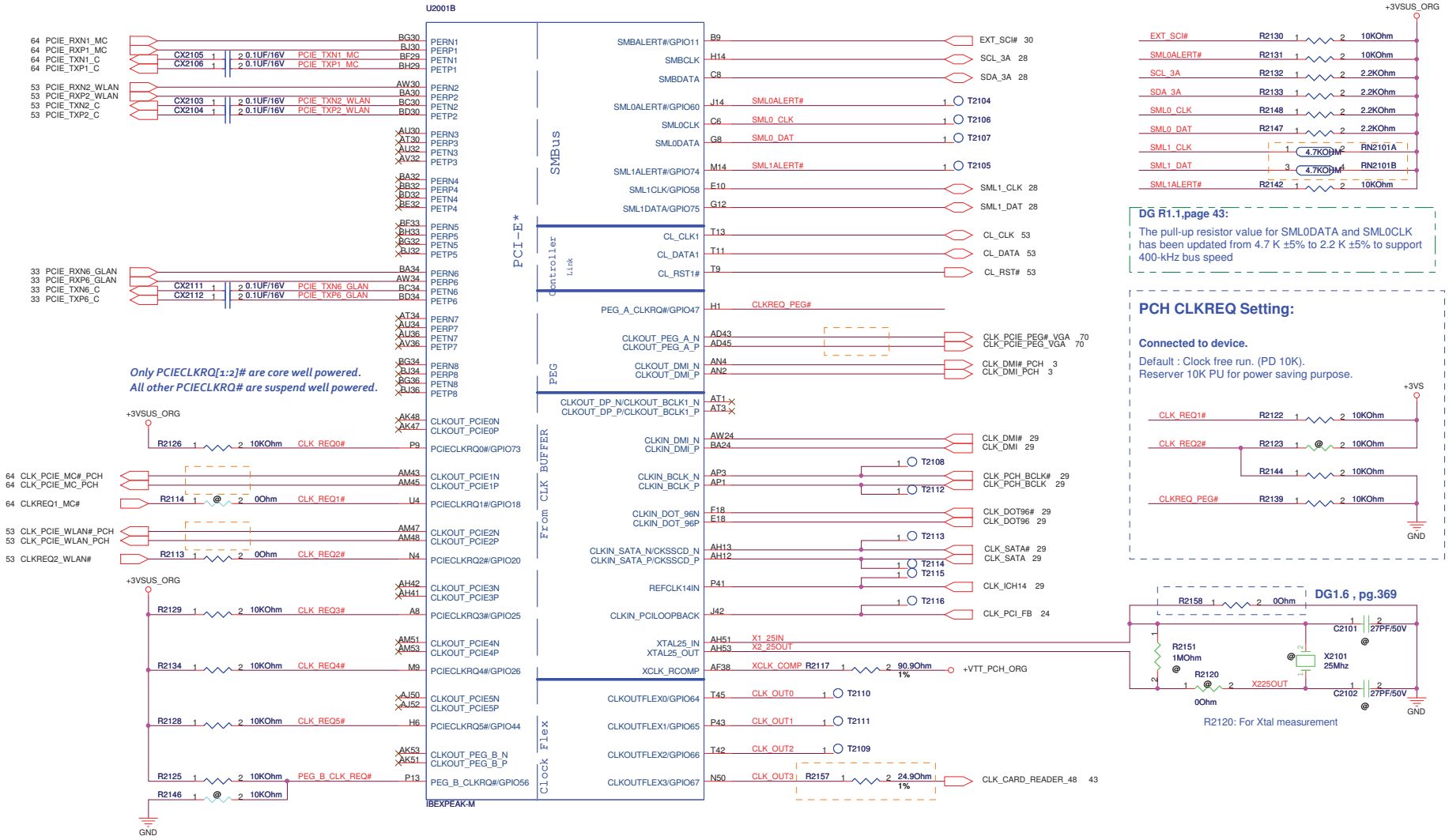
http://laptop-motherboard-schematic.blogspot.com/



		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

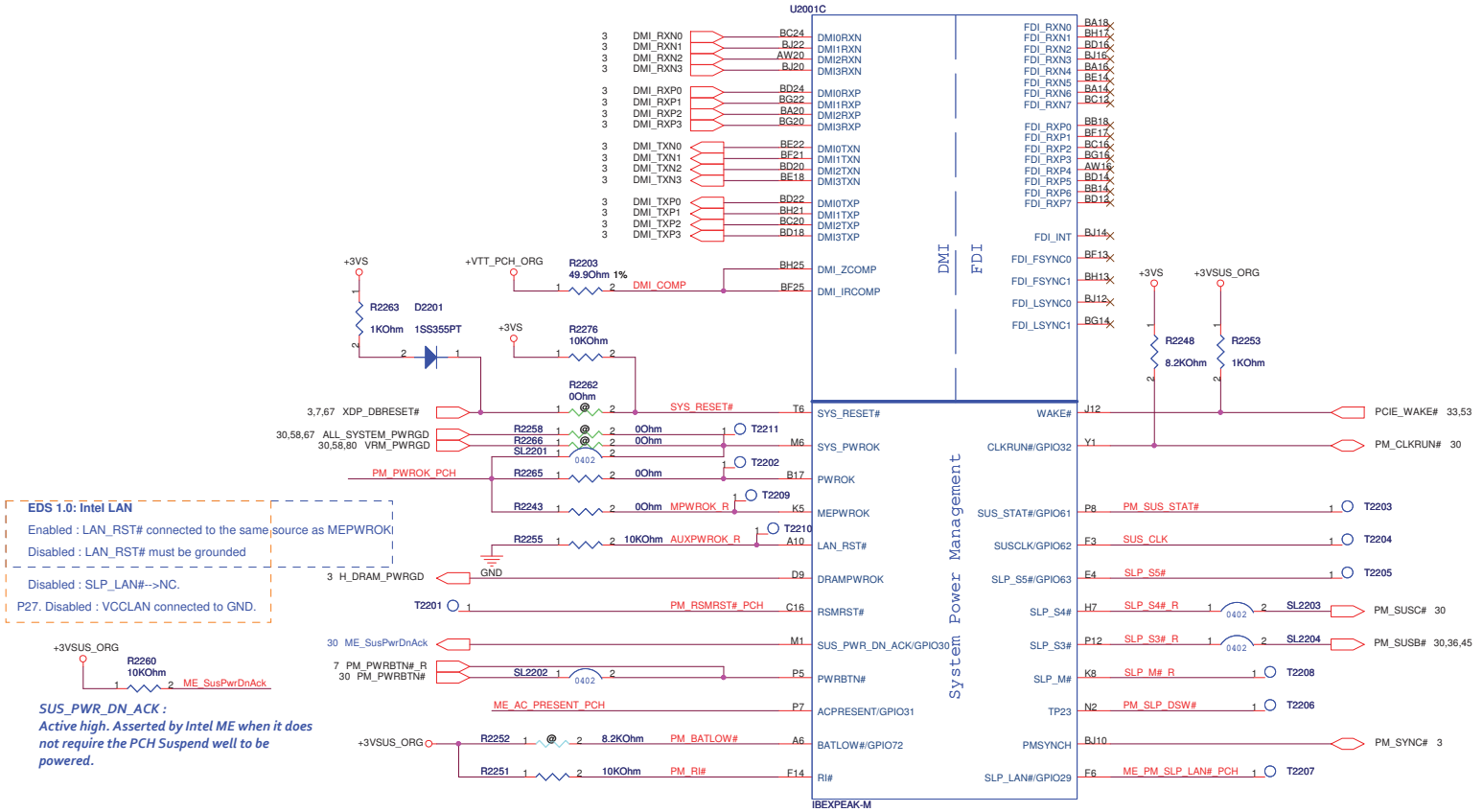
Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

http://laptop-motherboard-schematic.blogspot.com/



ASUSTeK COMPUTER INC. NB6	Title : PCH (2) PCIE,CLK	
	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 21 of 99	

http://laptop-motherboard-schematic.blogspot.com/



EDS 1.0: Intel LAN

Enabled : LAN_RST# connected to the same source as MEPWROK

Disabled : LAN_RST# must be grounded

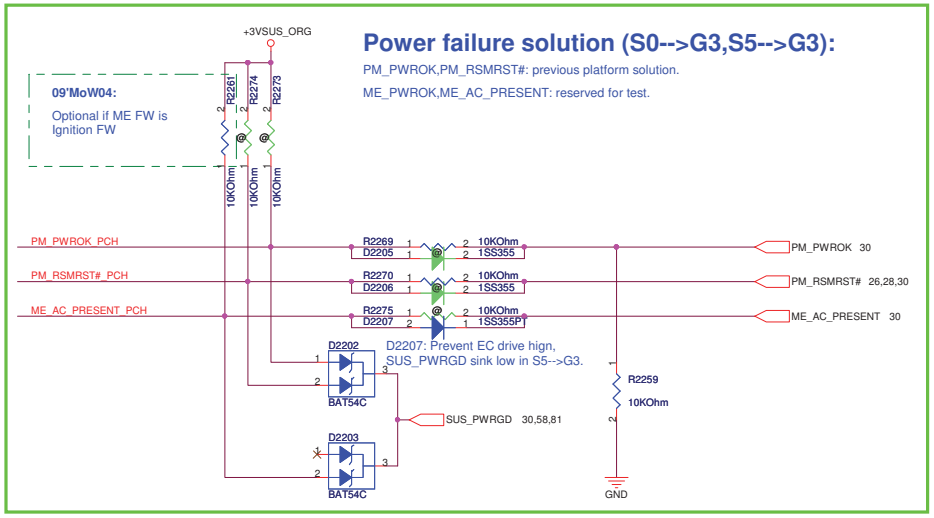
Disabled : SLP_LAN#-->NC.

P27. Disabled : VCCLAN connected to GND.

SUS_PWR_DN_ACK :
Active high. Asserted by Intel ME when it does not require the PCH Suspend well to be powered.

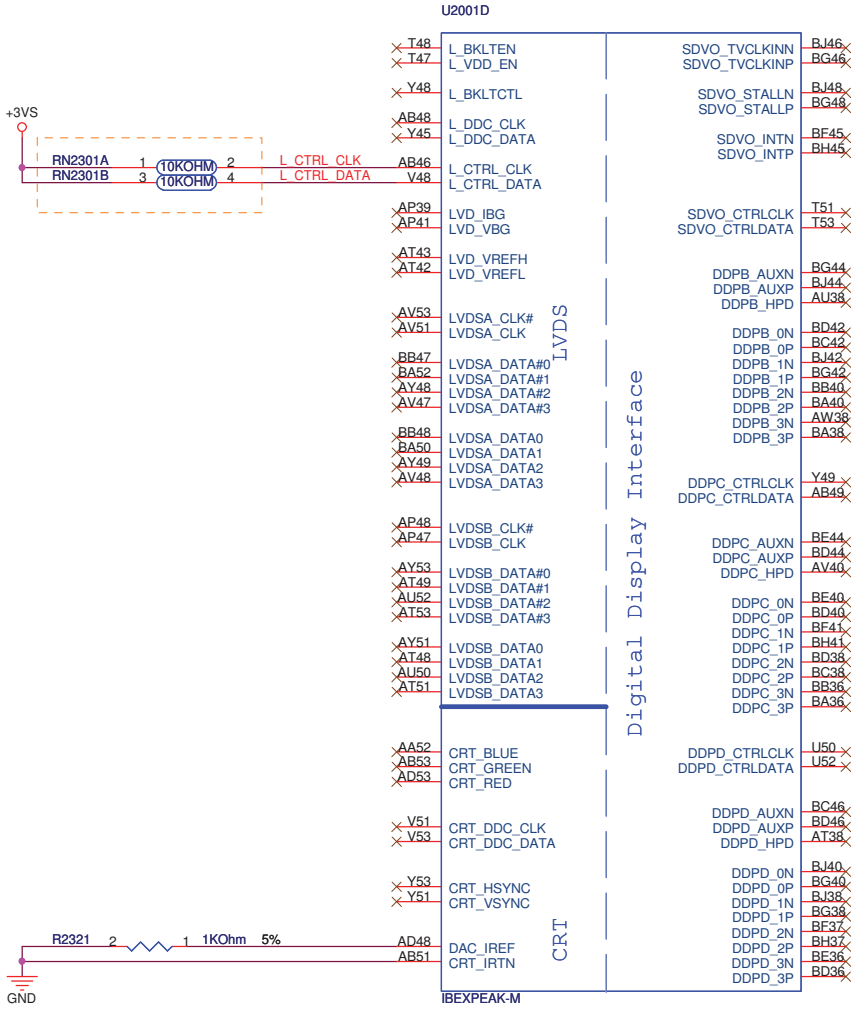
ACPRESENT :
Active high. Asserted by EC when the platform is connected to an AC source.

MoW 26 , 2009 :
The minimum time from WLAN device power valid until MEPWROK assertion is 20 mSecs.



ASUS	Title : PCH (3) FDI,DMI		
ASUSTeK COMPUTER INC. NB6	Engineer: Jerry Mou		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, December 11, 2009	Sheet 22 of 99		

http://laptop-motherboard-schematic.blogspot.com/



Port	Strap	How to enable the port	How to Disable the Port
LVDS	L_DDC_DATA	Pulled the signal high to 3.3V through 2.2K Ohm resistor	NC
Port B	SDVO_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm resistor	NC
Port C	DDPC_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm resistor	NC
Port D	DDPD_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm resistor	NC
eDP on CPU	CFG[4]	Pulled the signal down to the GND through a 3.3K ohm resistor	NC

ASUS

Title : PCH - LVDS,CRT

ASUSTeK COMPUTER INC. NB6

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	K72Jr	2.0

Date: Friday, December 11, 2009 Sheet 23 of 99

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GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap		
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.

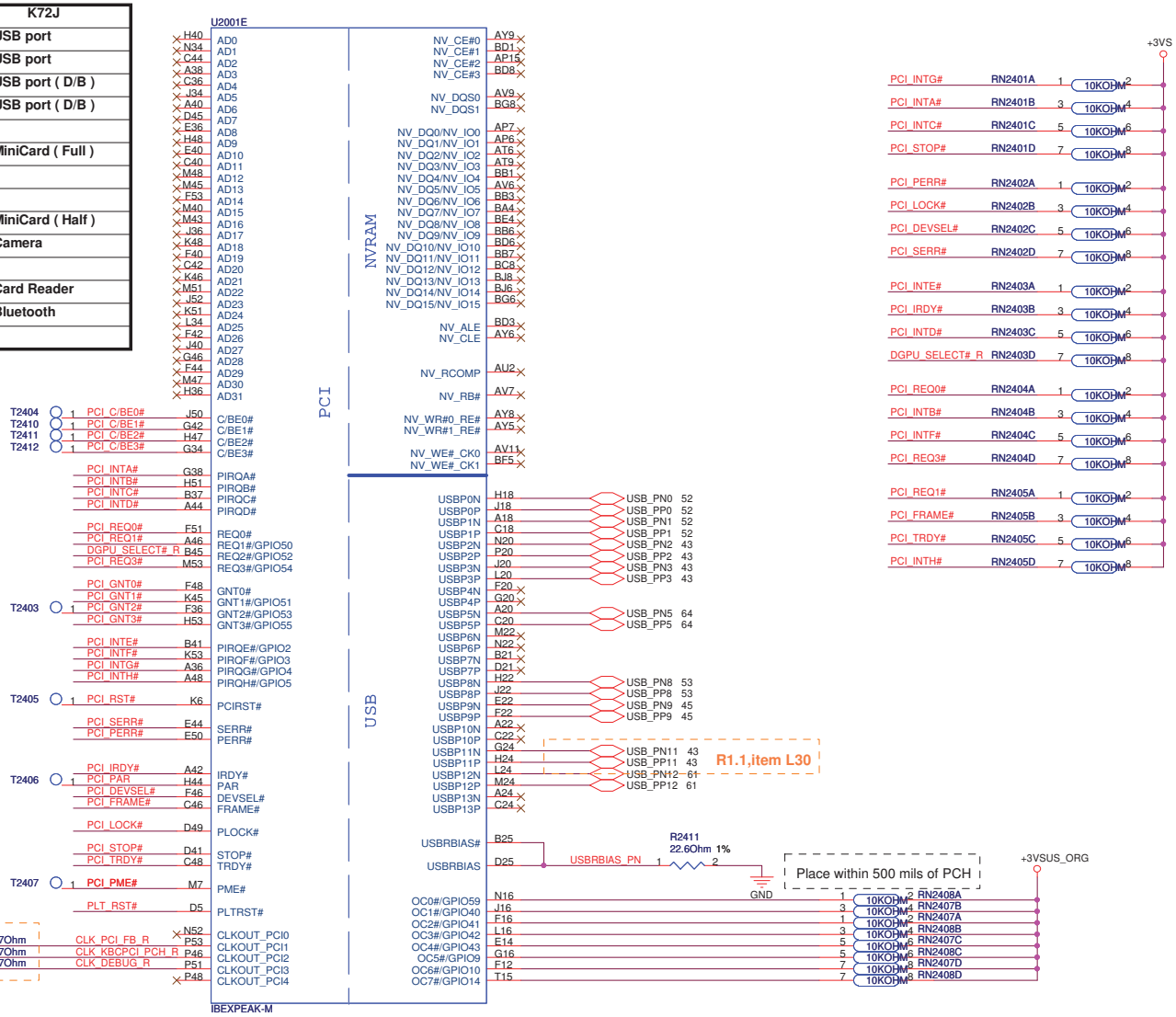
PCI_GNT0# R2440 1 @ 2 1KOhm
PCI_GNT1# R2441 1 @ 2 1KOhm
GND

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

PCI_GNT3# R2444 1 @ 2 1KOhm
GND

	K72J
0	**USB port**
1	**USB port**
2	**USB port (D/B)**
3	**USB port (D/B)**
4	
5	**MiniCard (Full)**
6	
7	
8	**MiniCard (Half)**
9	**Camera**
10	
11	**Card Reader**
12	**Bluetooth**
13	



MoW 02 , 2009
Intel recommends that customers do not perform USB or SATA Signal Quality testing at this time. Ibex Peak Sightings Report Rev. 004 contains a new sighting about USB Eye Diagram Failure. A similar sighting about SATA will be available in the next sightings report release. Customers may begin Signal Quality testing on PCIe.

ASUS	Title : PCH - PCI,USB	
ASUSTeK COMPUTER INC. NB6	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 24 of 99	

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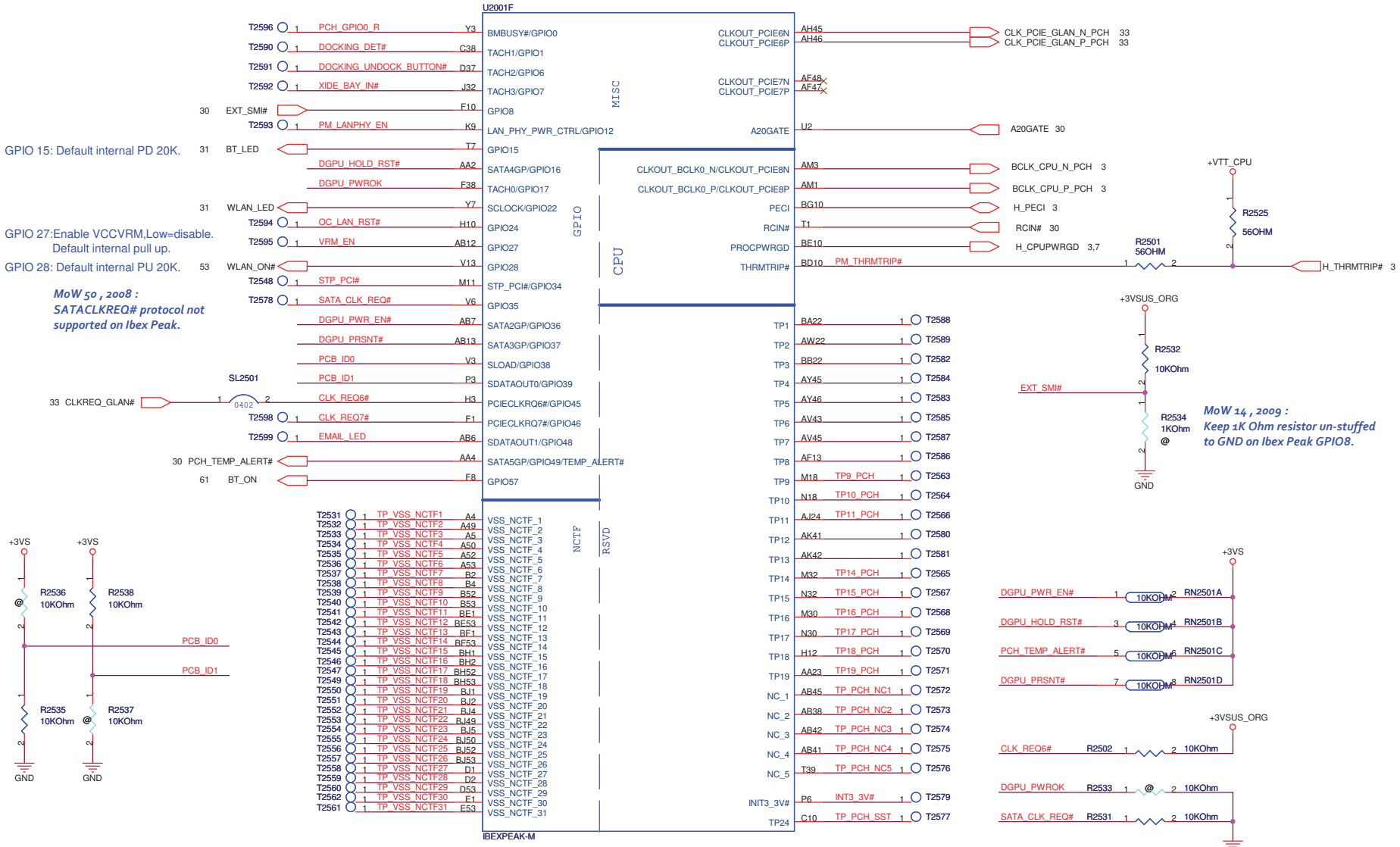
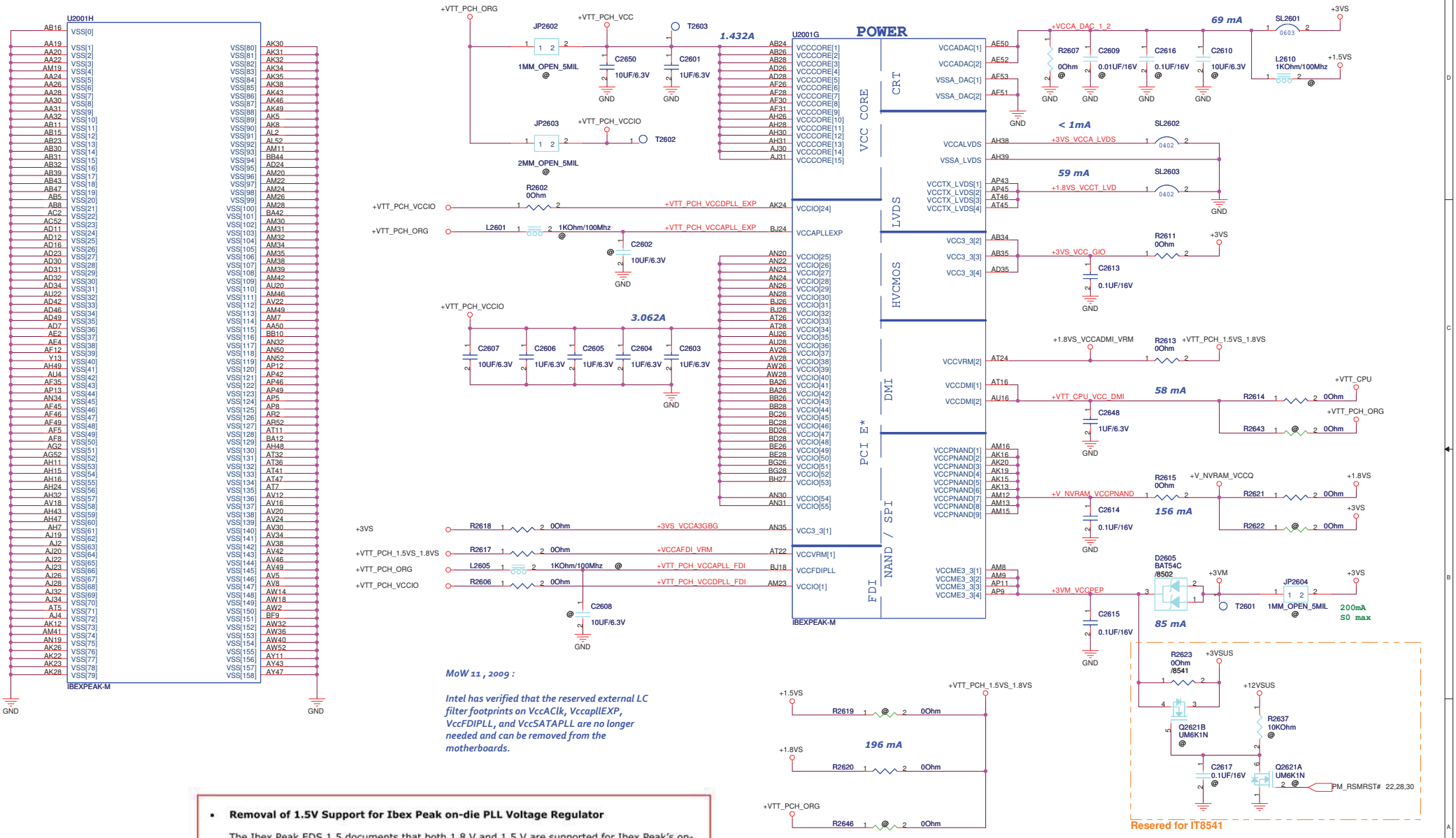
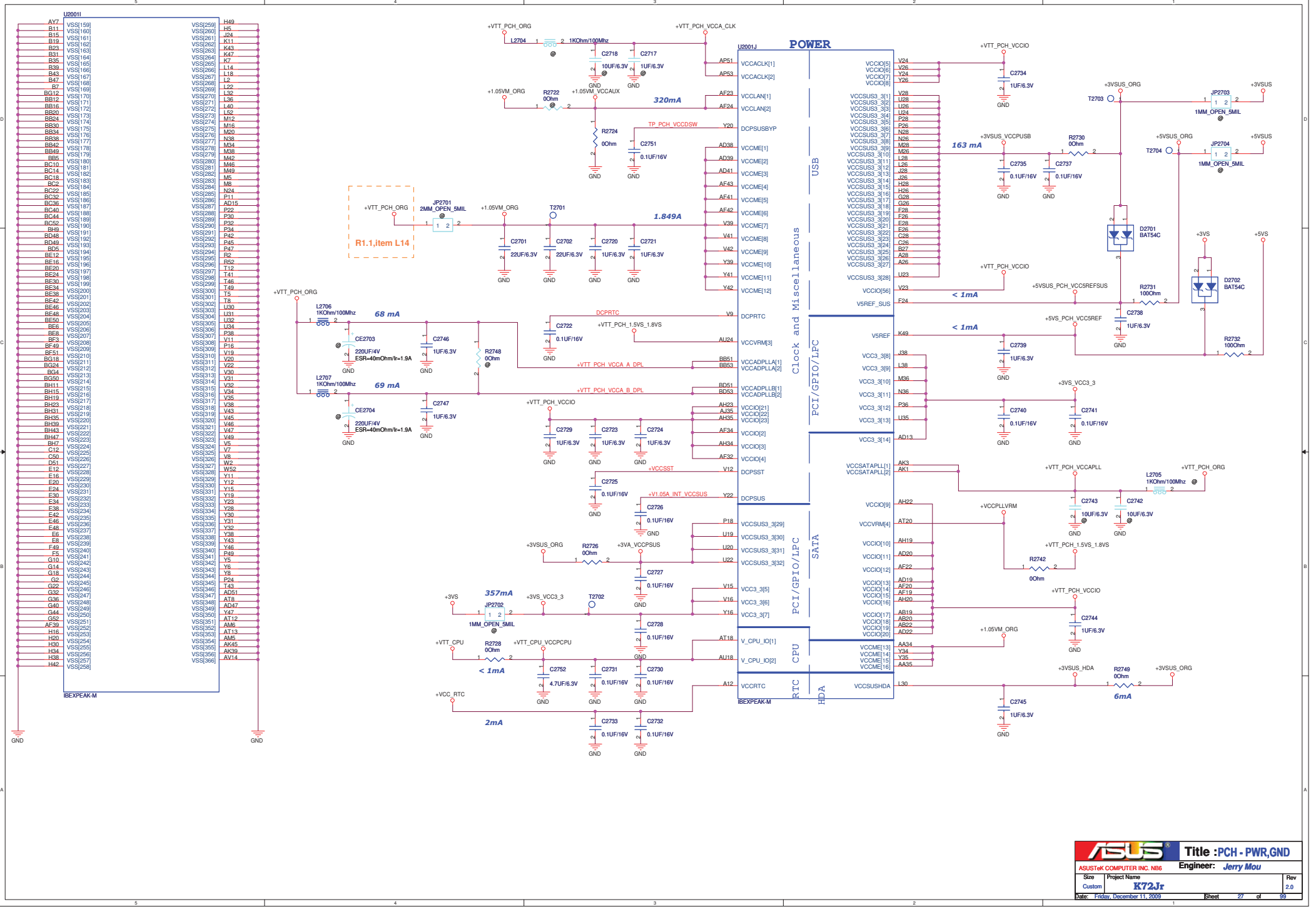


ASUSTeK COMPUTER INC. NB6	Title : PCH - CPU,GPIO	Engineer: Jerry Mou
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, January 22, 2010	Sheet 25 of 99	

http://laptop-motherboard-schematic.blogspot.com/

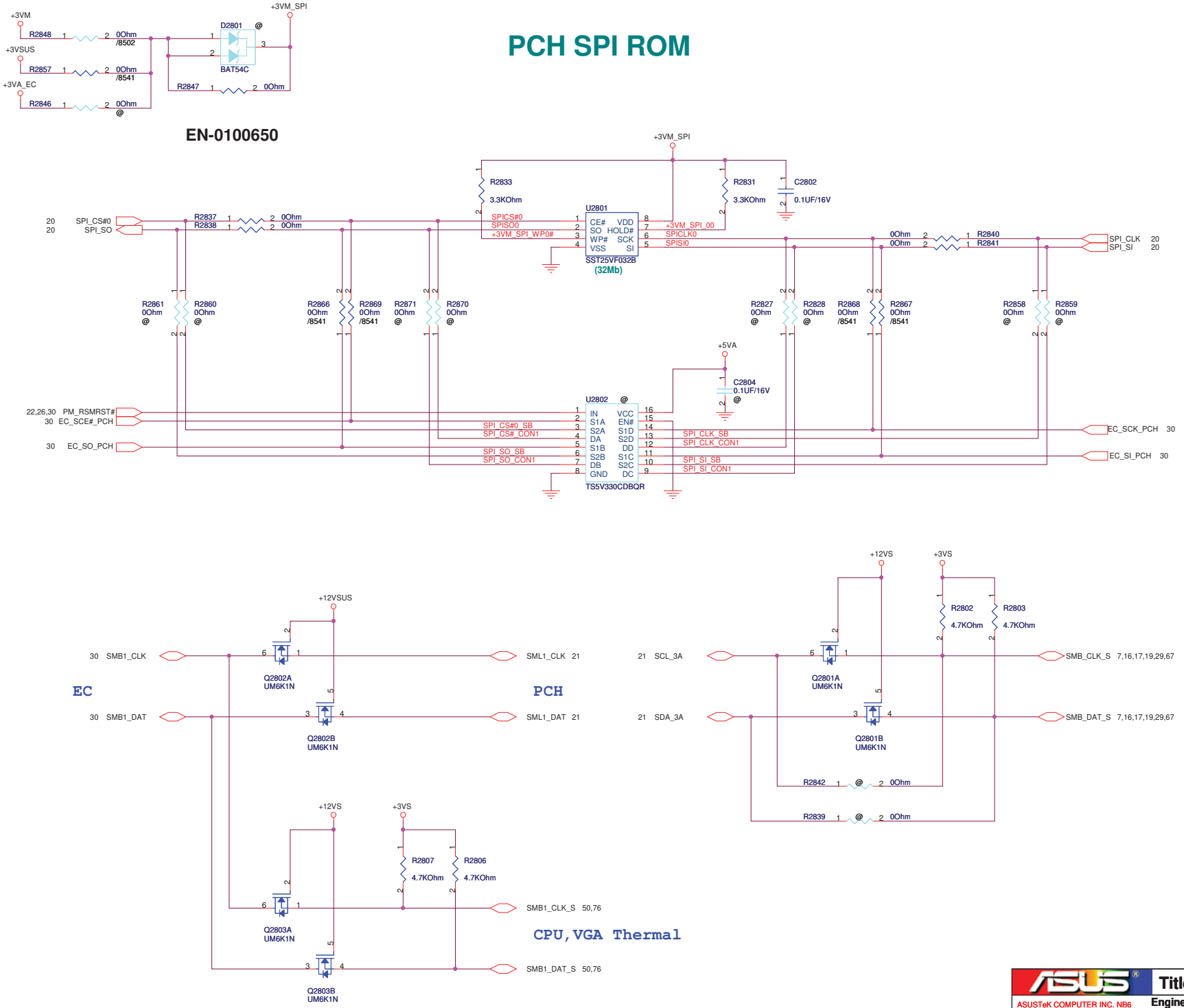


http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

PCH SPI ROM



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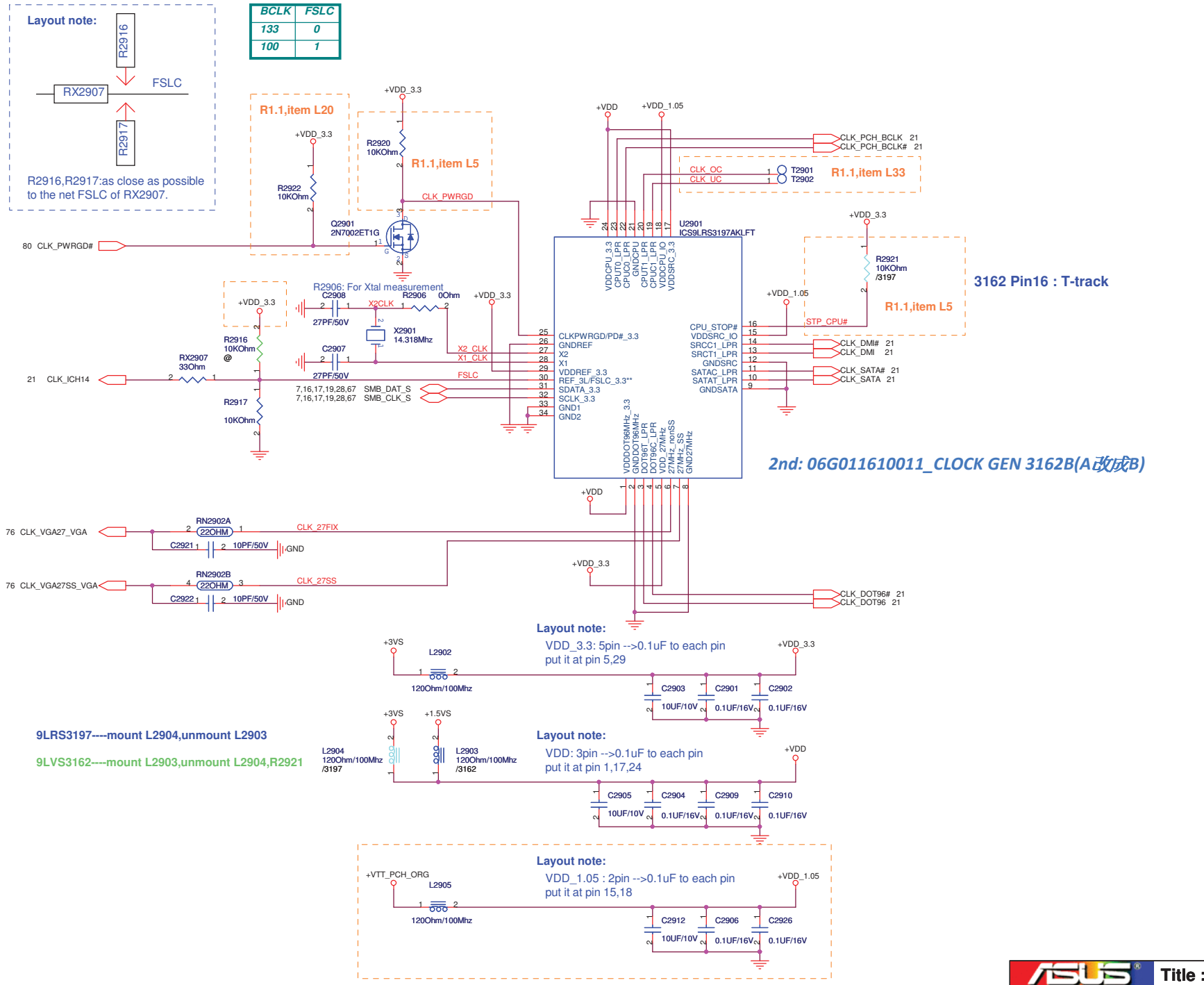
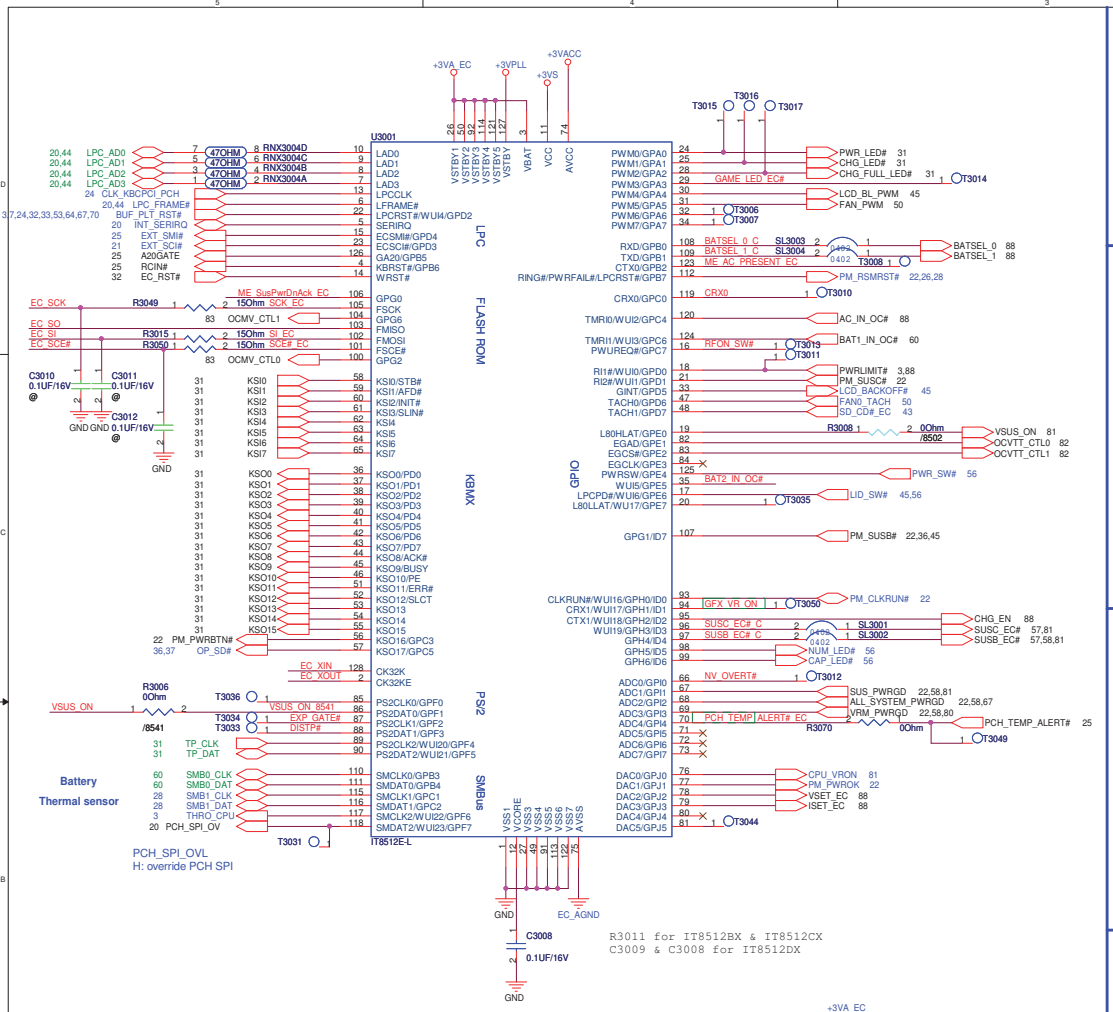
ASUS	Title : PCH_SPI ROM	
ASUSTeK COMPUTER INC. NB6	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 28 of 99	

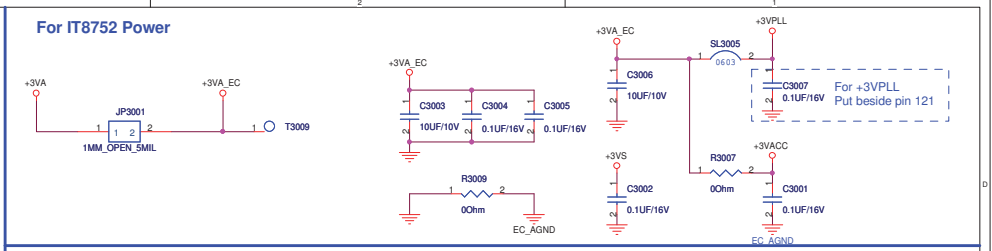


http://laptop-motherboard-schematic.blogspot.com/

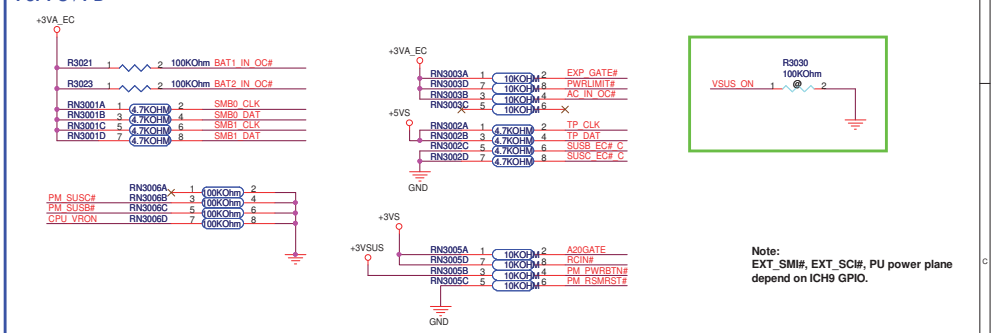
ASUSTeK COMPUTER INC. NB4	Title : CLK_ICS9LRS3197		
	Engineer: Jerry Mou		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, January 22, 2010	Sheet 29 of 100		



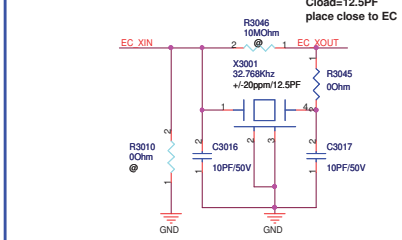
For IT8752 Power



For PU / PD



For X'tal



For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

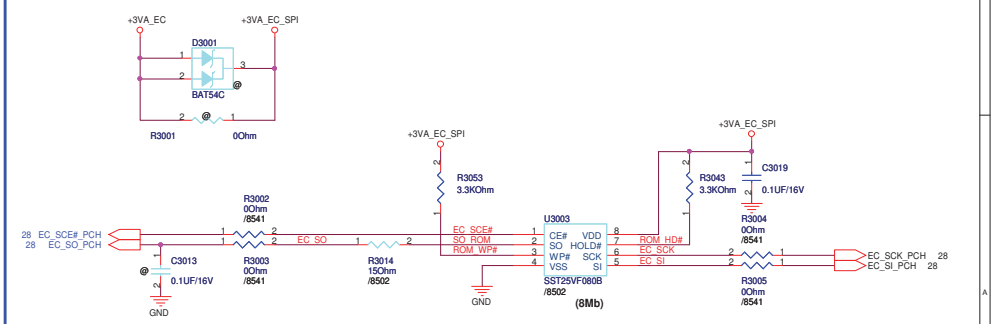
Note: It can be programmable by EC fireware.

PP Enable

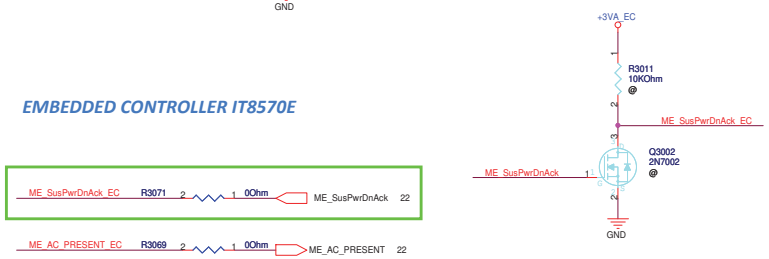
Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

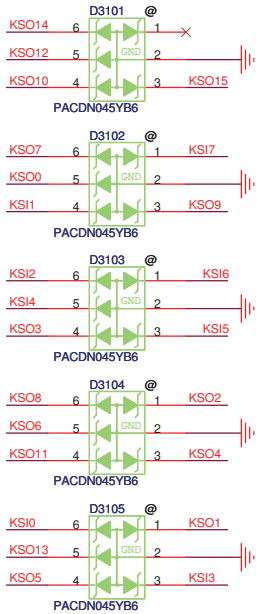


06G042030010 **EMBEDDED CONTROLLER IT8570E**

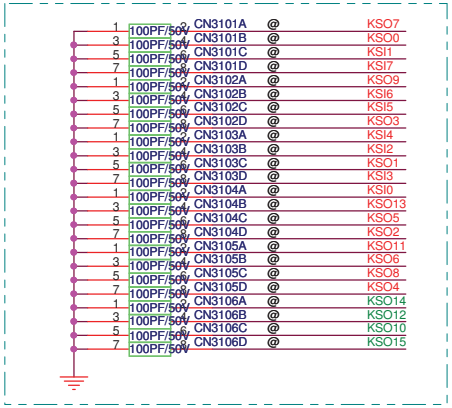


ASUS / ASUSTeK COMPUTER INC. NB4	Title : EC_IT8541		
	Engineer: Jerry Mou		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, December 11, 2009	Sheet 30 of 100		

http://laptop-motherboard-schematic.blogspot.com/

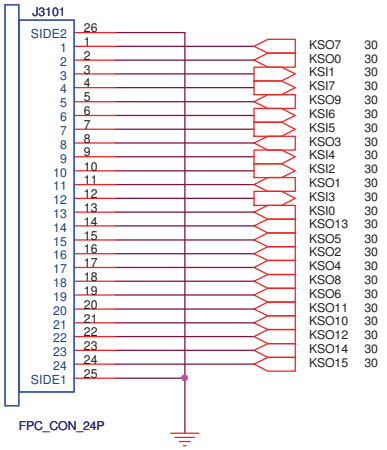


EMI



Keyboard

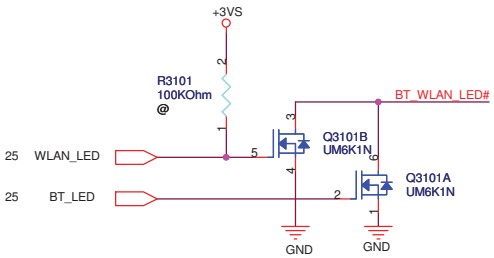
TOP connector 下接觸
PIN1上面 KSO7 ;下面 KSO24

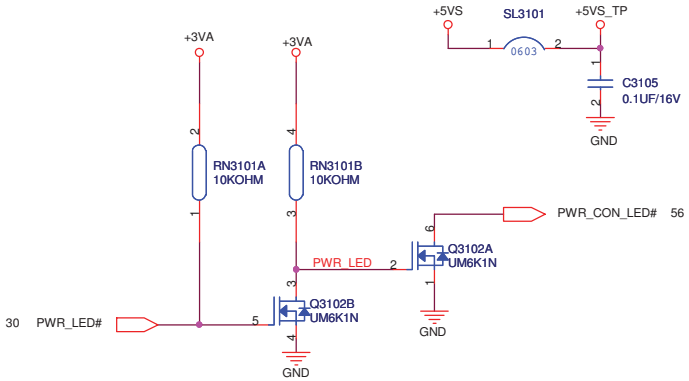


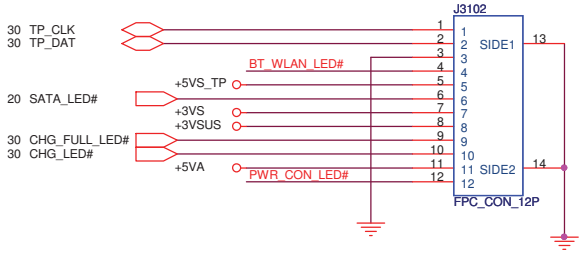
12G182102402

12 Pin Touch-Pad Conn.

TP M/B TOP 上接觸 PIN1 左邊 CLK ; TP SMALL BOTTOM 下接觸. Cable 折兩次







12G18340120C

ASUS	Title : EC_IT8541(2/2)KB, TP		
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang		
Size B	Project Name K72Jr		Rev 2.0
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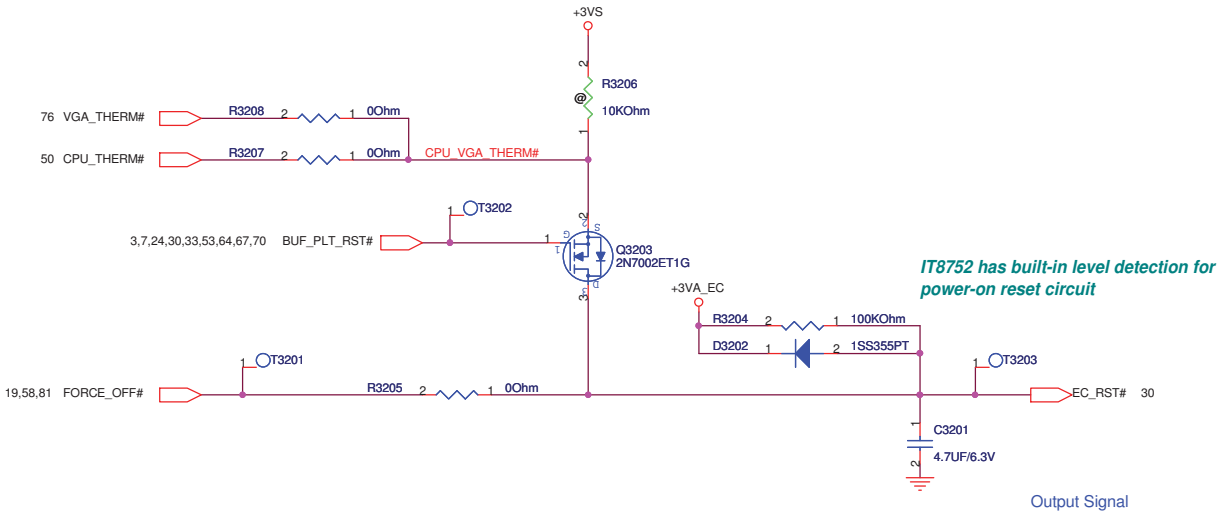
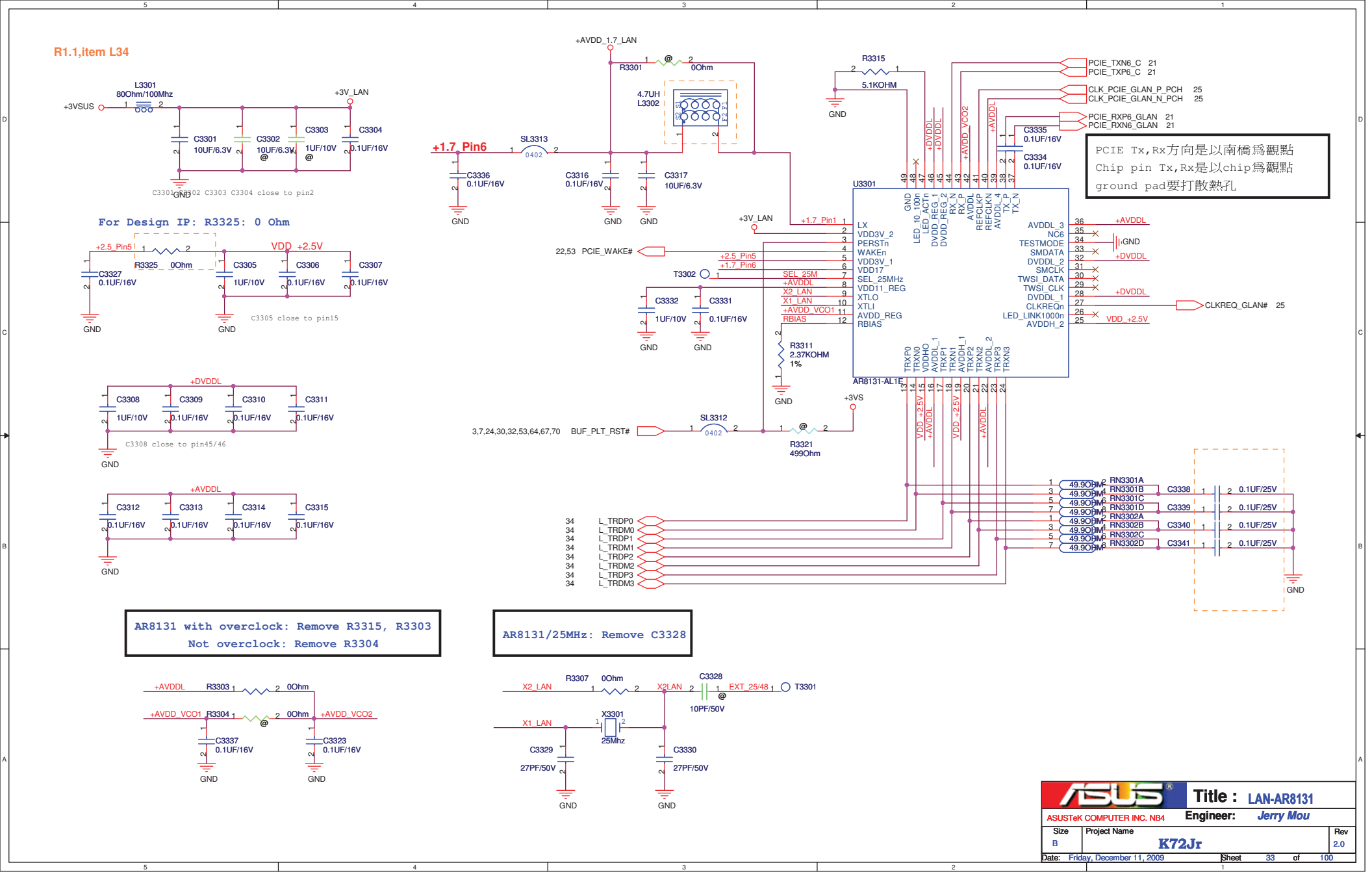
Thermal Policy



ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: Jerry Mou	
Size B	Project Name K72Jr	Rev 2.0
Date: Friday, December 11, 2009	Sheet 32 of 100	

http://laptop-motherboard-schematic.blogspot.com/



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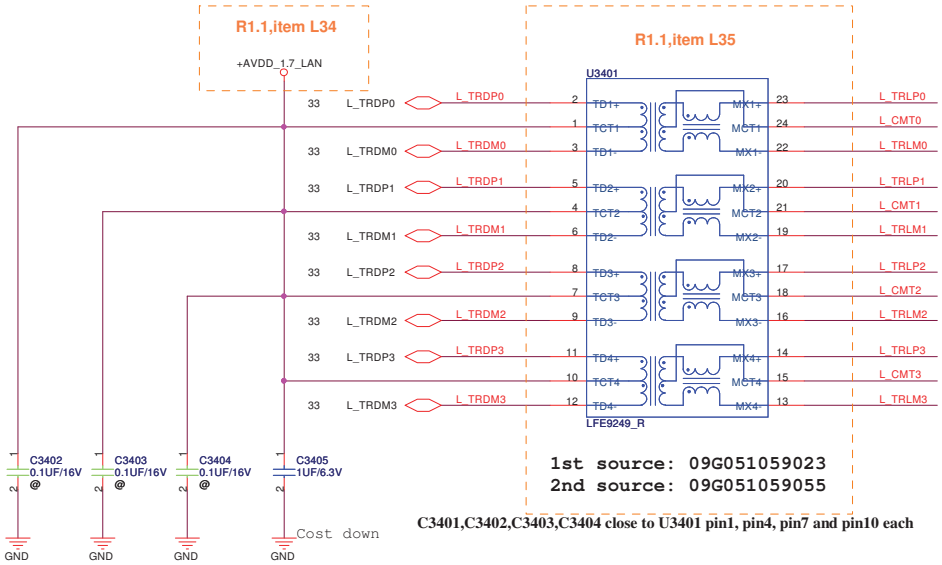
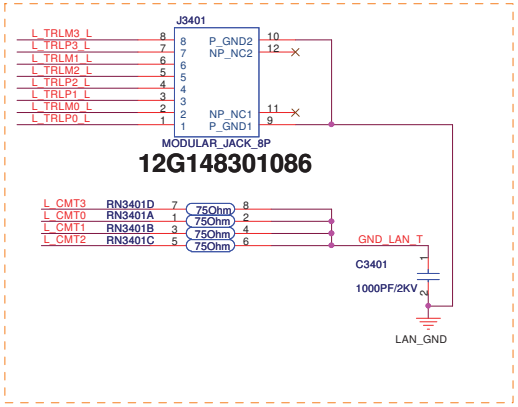
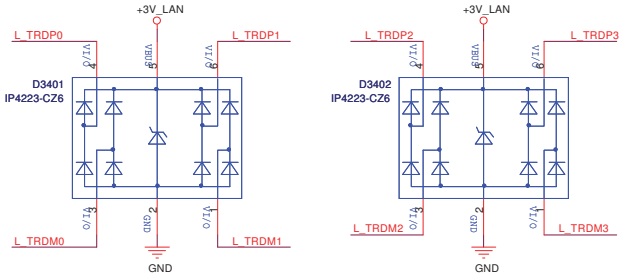


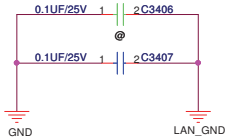
1st source: 09G051059023
2nd source: 09G051059055

C3401,C3402,C3403,C3404 close to U3401 pin1, pin4, pin7 and pin10 each

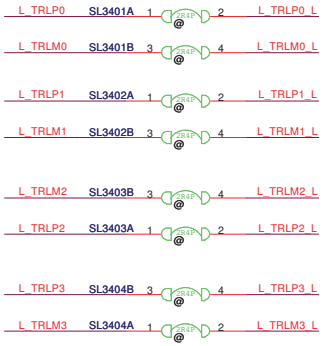
connector without modem







Place near chassis GND



ASUS	Title : LAN_RJ45	
ASUSTeK COMPUTER INC. NB4	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 34 of 100	

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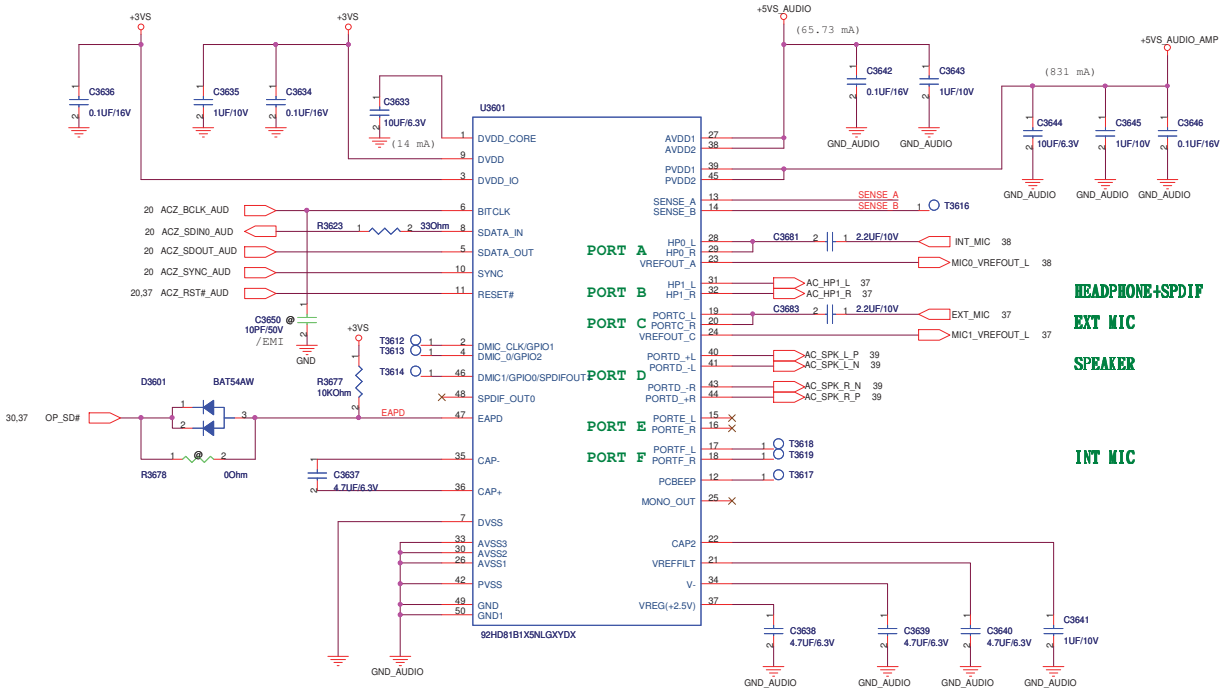
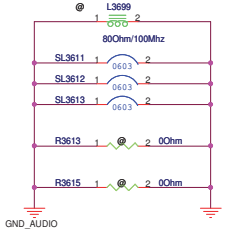
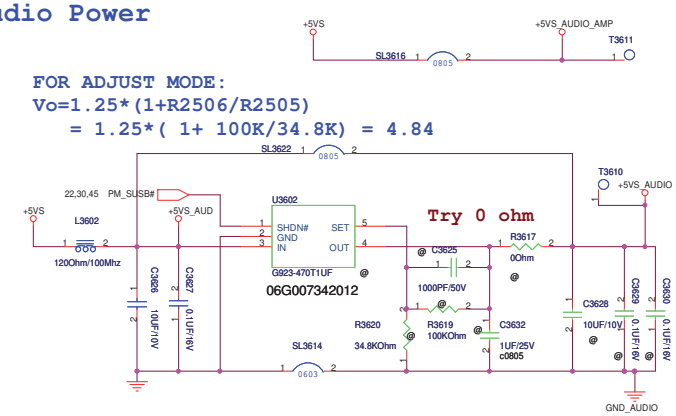
ASUSTeK COMPUTER INC. NB4	Title : MDC_****	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
Date: Friday, December 11, 2009	Sheet 35 of 100	

http://laptop-motherboard-schematic.blogspot.com/

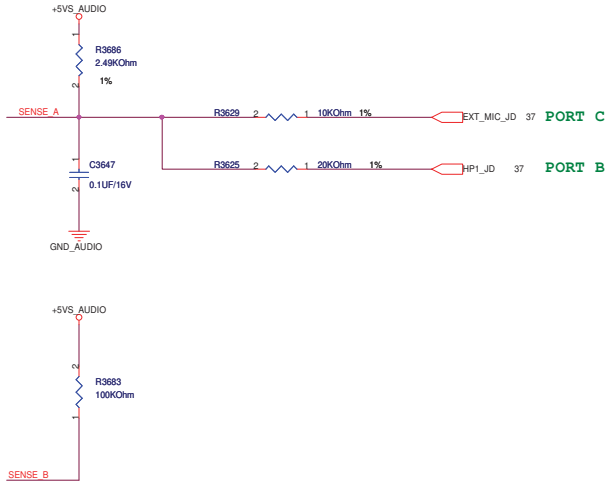




Audio Power



SENSE



PC BEEP

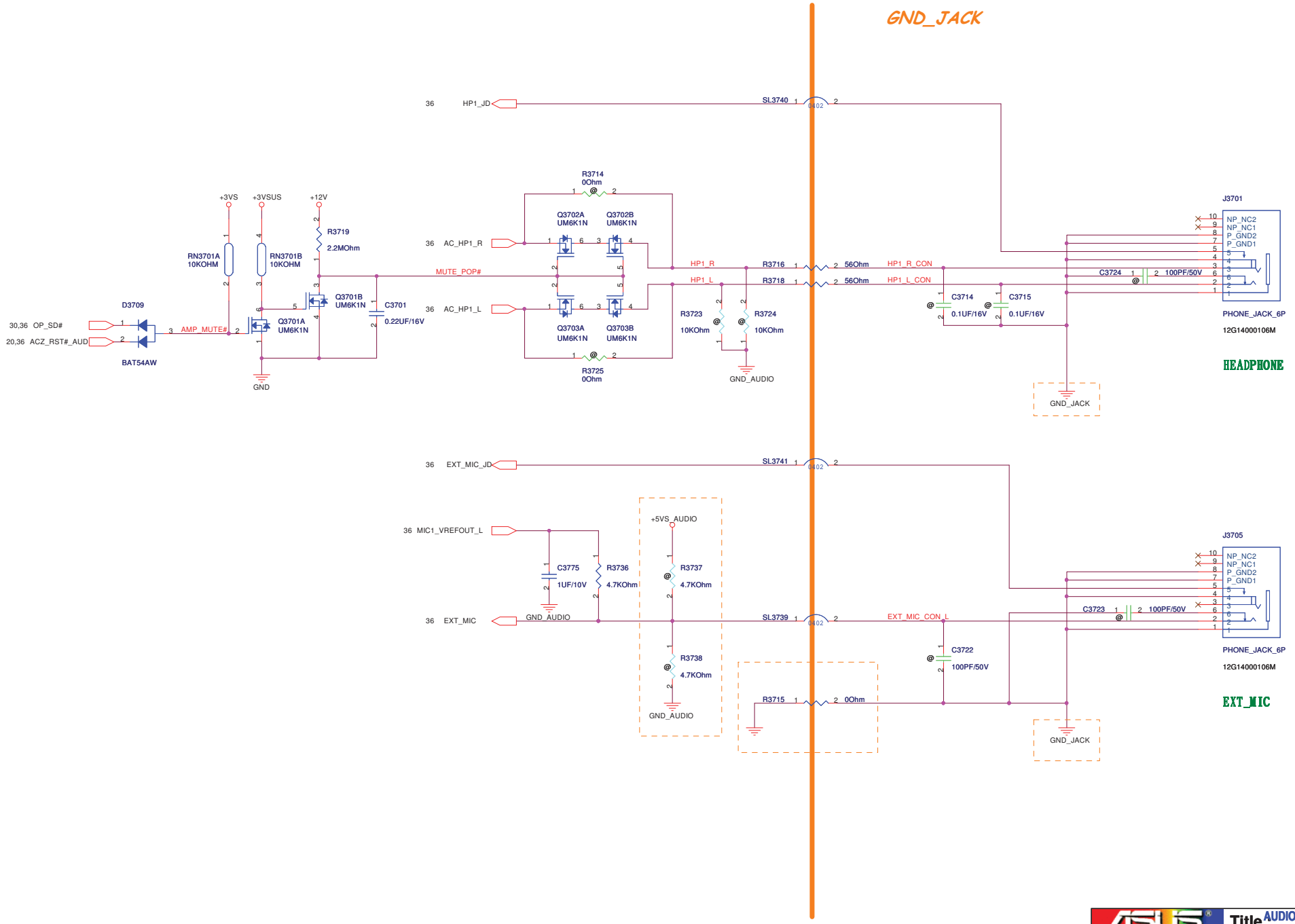
Remove PC_BEEP Circuit 2009/06/16

Please remove the PC Beep function from Verb table.

<Variant Name>

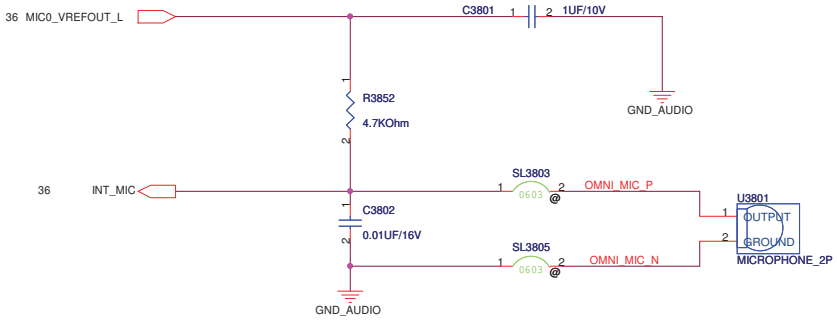
ASUS	Title : CODEC IDT92HD81	
ASUSTeK COMPUTER INC. NB2	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 36 of 100	

http://laptop-motherboard-schematic.blogspot.com/



ASUS	Title: AUDIO AMP & JACK	
ASUSTeK COMPUTER INC. NB2	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 37 of 100	

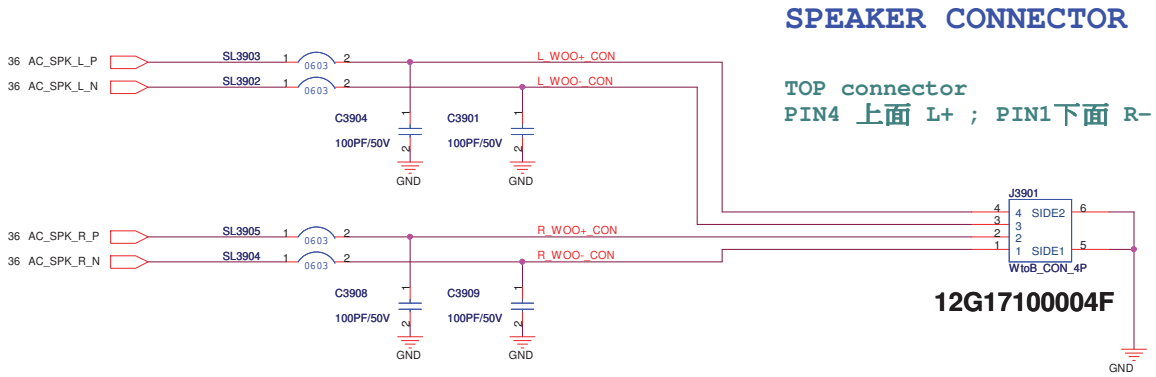
http://laptop-motherboard-schematic.blogspot.com/



<Variant Name>

ASUSTeK COMPUTER INC. NB2	Title : AUD_I_MIC		
	Engineer: Jerry Mou		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, December 11, 2009	Sheet 38 of 100		

http://laptop-motherboard-schematic.blogspot.com/



ASUSTeK COMPUTER INC. NB4	Title : AUD_Woofer	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 39 of 100	

http://laptop-motherboard-schematic.blogspot.com/

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: C	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 40 of 100	

http://laptop-motherboard-schematic.blogspot.com/

Main Board

ASUSTeK COMPUTER INC. NB4	Title : CB_****	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
Date: Friday, December 11, 2009	Sheet 41 of 100	

http://laptop-motherboard-schematic.blogspot.com/

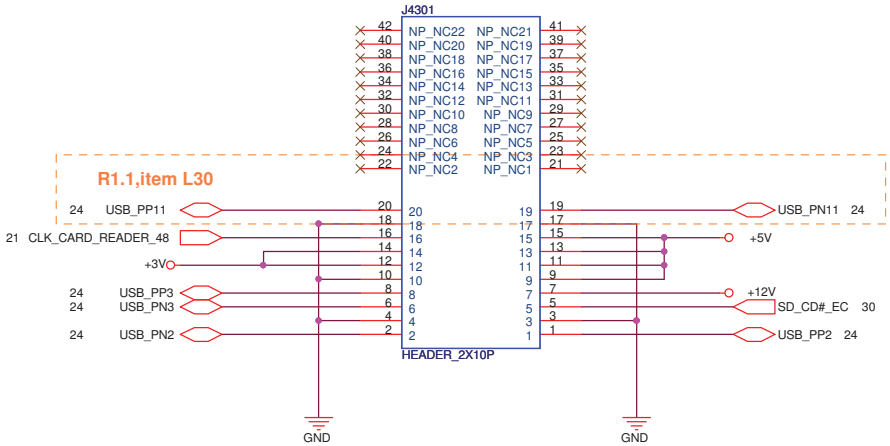
Main Board

ASUSTeK COMPUTER INC. NB4	Title : CB_****	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
Date: Friday, December 11, 2009	Sheet 42 of 100	

http://laptop-motherboard-schematic.blogspot.com/

K72J USB Board_20 Pin CON

TOP connector
左上 PIN20 USB_PP4 ; 右上 PIN19 USB_PN4
左下 PIN2 USB_PN2 ; 右下 PIN1 USB_PP2

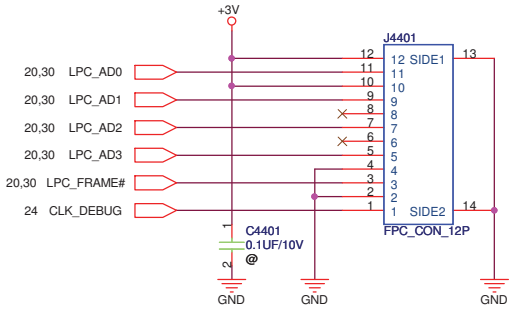


2nd : 12G06120020A

ASUS	Title :	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
Date: Friday, December 11, 2009	Sheet 43 of 100	

http://laptop-motherboard-schematic.blogspot.com/

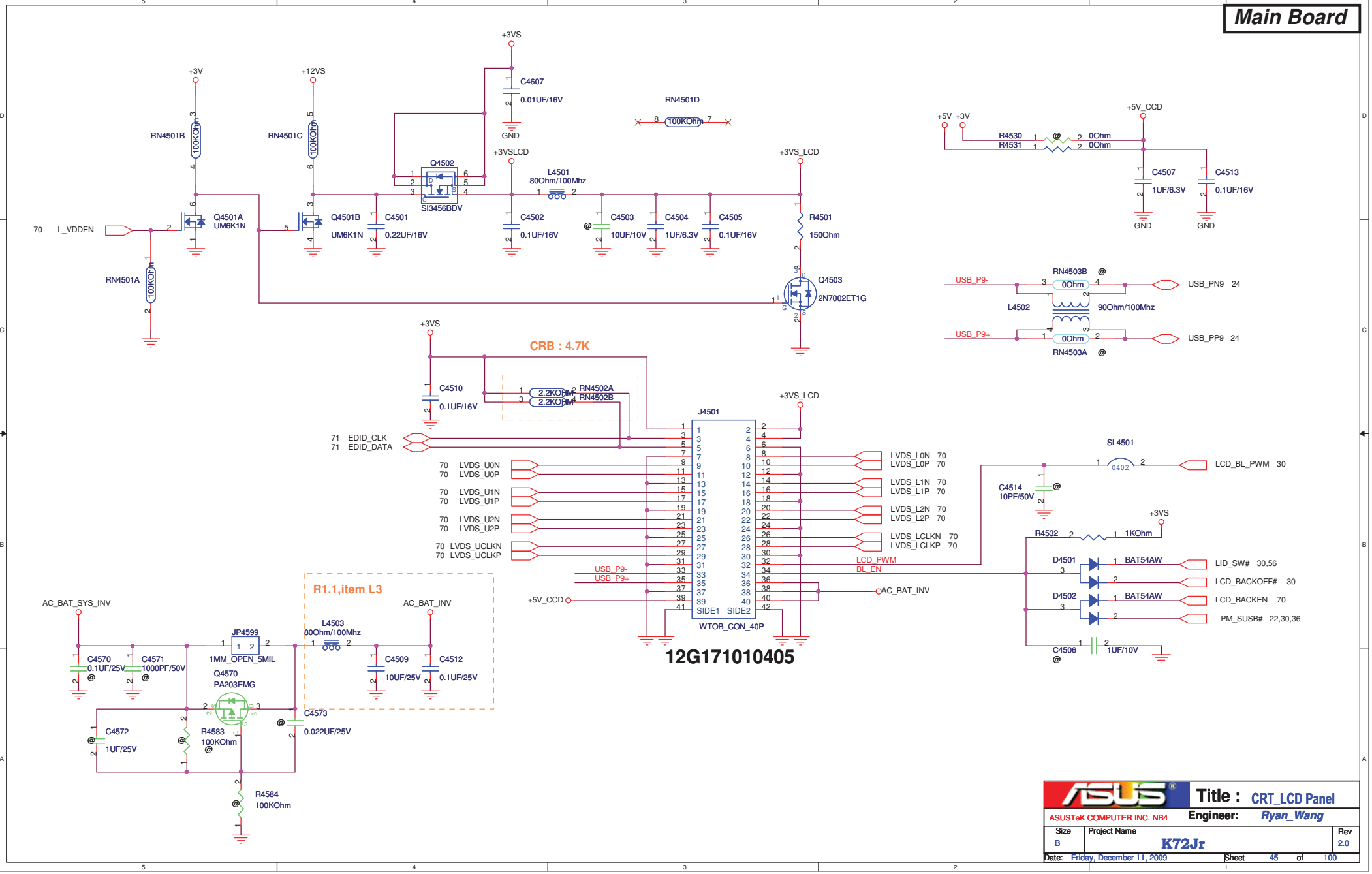
LPC Debug Port



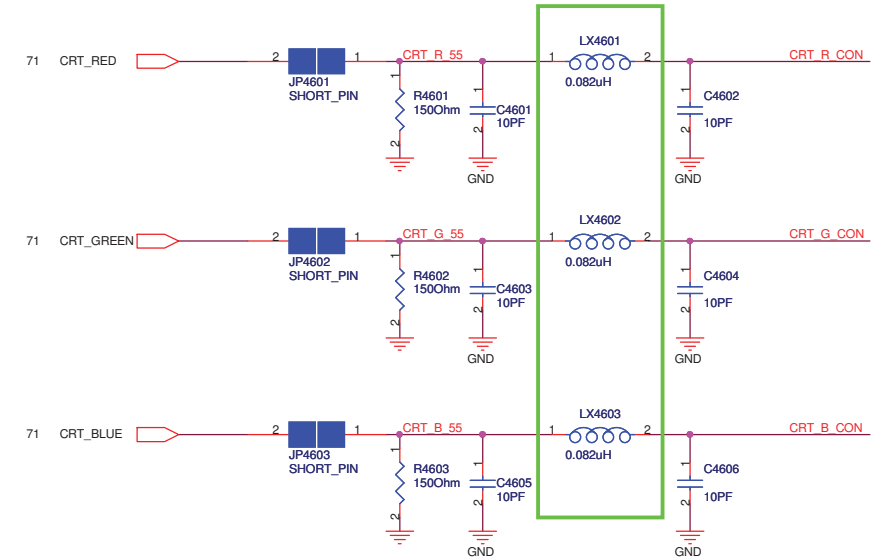
TP M/B TOP 下接觸 PIN1 上面 CLK ; Pin 12 下面 +3V

ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
Date: Friday, December 11, 2009	Sheet 44 of 100	

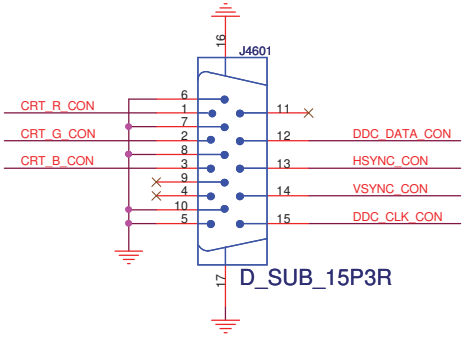
http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

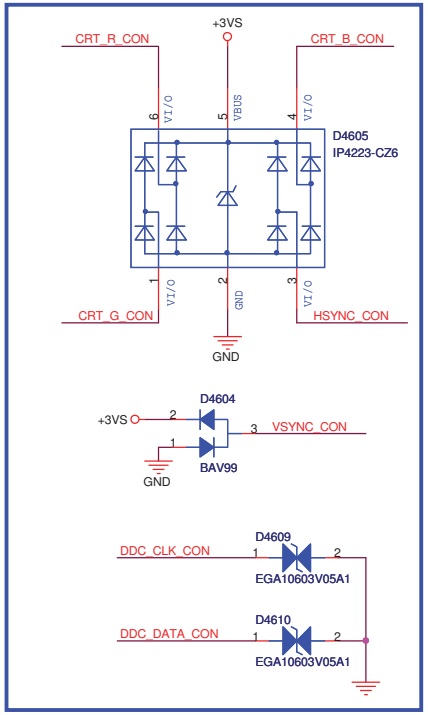


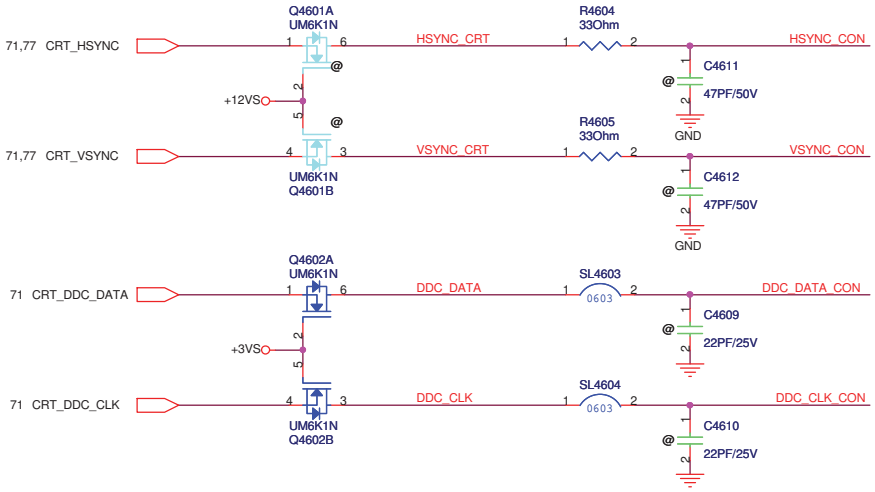
09G013047105

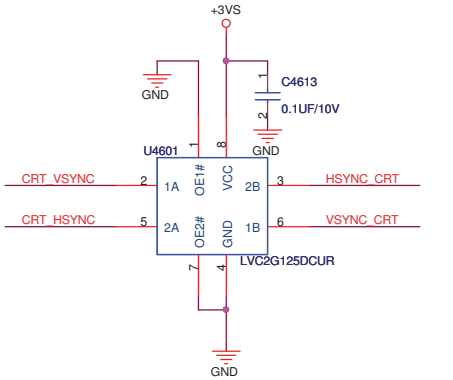


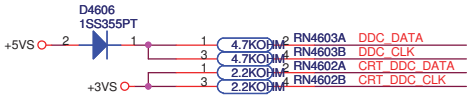
12G101102155

PLACE ESD Diodes near connector







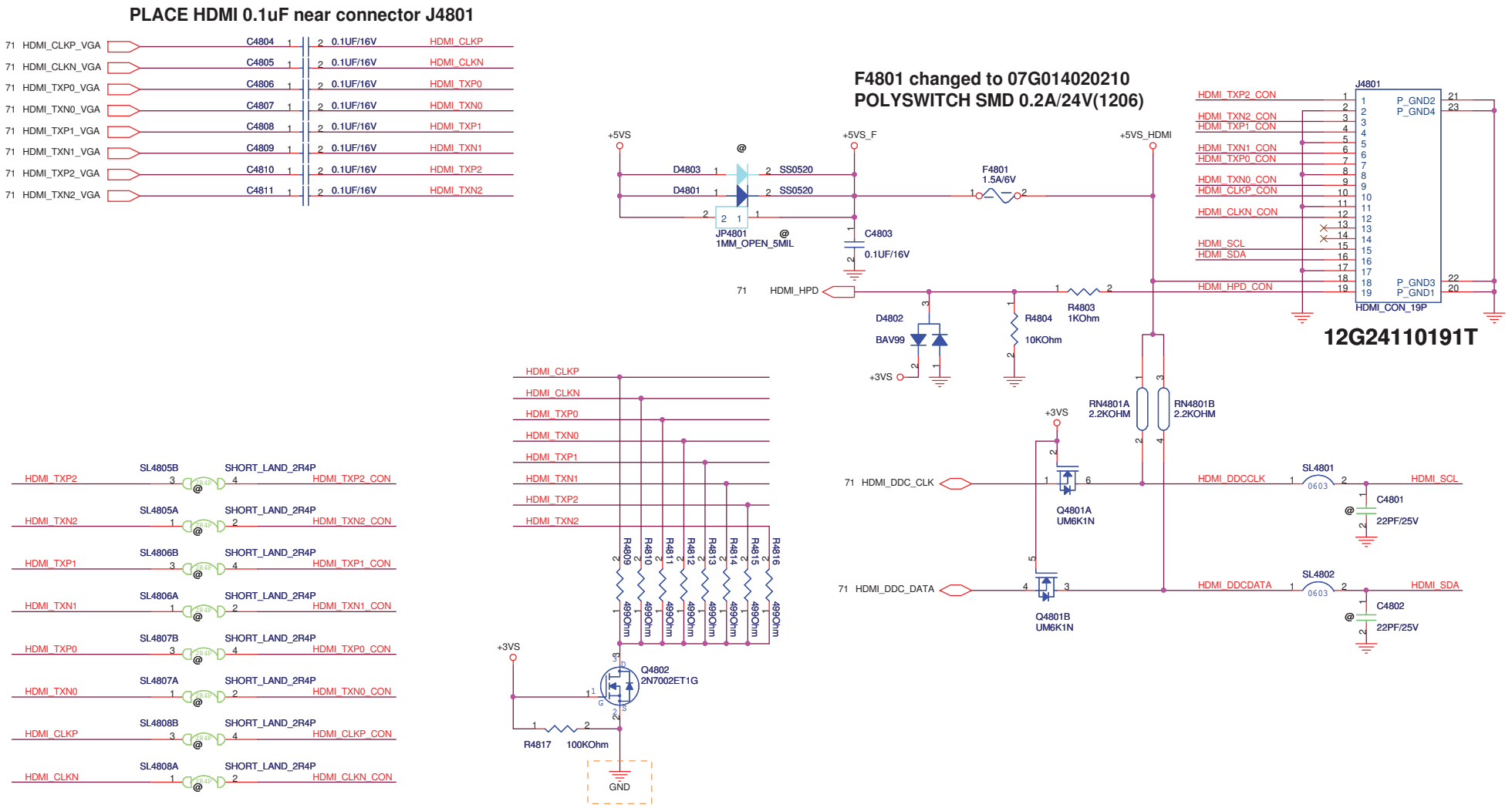


ASUS	Title : CRT_D-Sub		
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang		
Size B	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009	Sheet 46 of 100		

http://laptop-motherboard-schematic.blogspot.com/

ASUSTeK COMPUTER INC. NB4	Title :	
	Engineer: Ryan_Wang	
Size: C	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 47 of 100	

http://laptop-motherboard-schematic.blogspot.com/



ASUS	Title : TV_HDMI	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
Date: Monday, February 01, 2010	Sheet 48 of 100	

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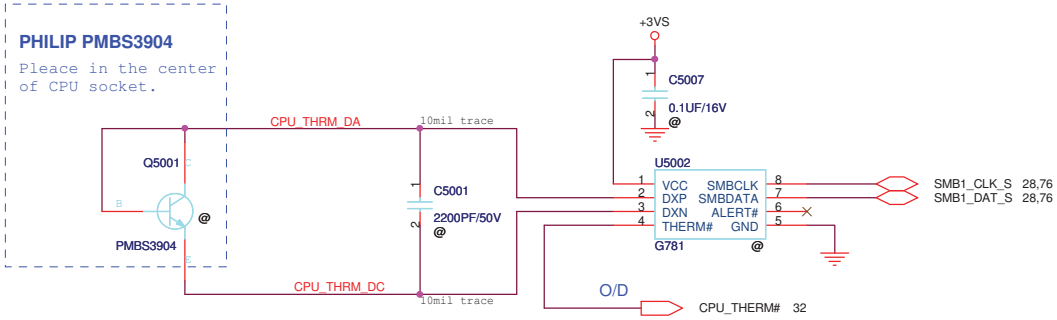
Main Board

ASUSTeK COMPUTER INC. NB4	Title : TV_****	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
Date: Friday, December 11, 2009	Sheet 49 of 100	

http://laptop-motherboard-schematic.blogspot.com/

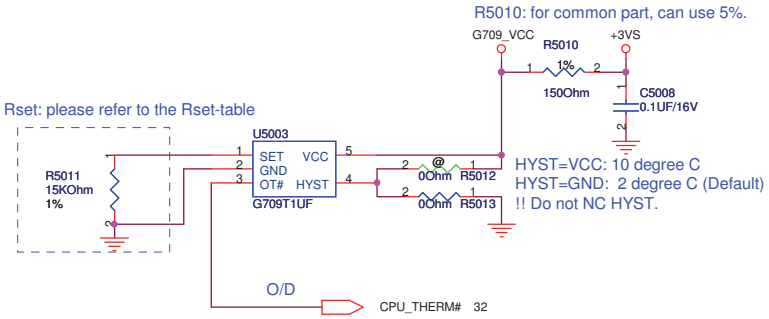
CPU Thermal Sensor



SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

CPU Thermal Sensor



Layout note:

Place U5003 at the center of the CPU socket.

Rset(Kohm)=0.0012T*T-0.9308*T+96.147

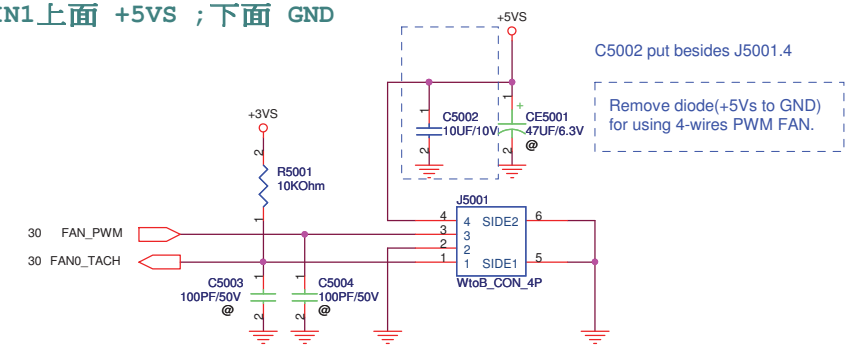
Resistor Accuracy: +/- 1%

G709 Temperature Threshold Accuracy: -4.7 degree C ~ +4.7 degree C

Set center temperature=96.06 degree C
Rset value is depend on thermal request.
For M60J,possible board shutdown temperature: 91 ~ 101 degree C.

PWM Fan

BOTTOM connector
PIN1上面 +5VS ;下面 GND

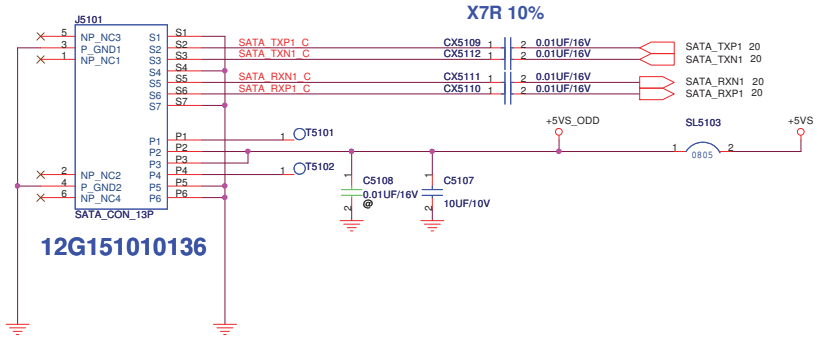


12G17000004B

ASUS	Title : FAN_Fan & Sensor	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
Date: Friday, December 11, 2009	Sheet 50 of 100	

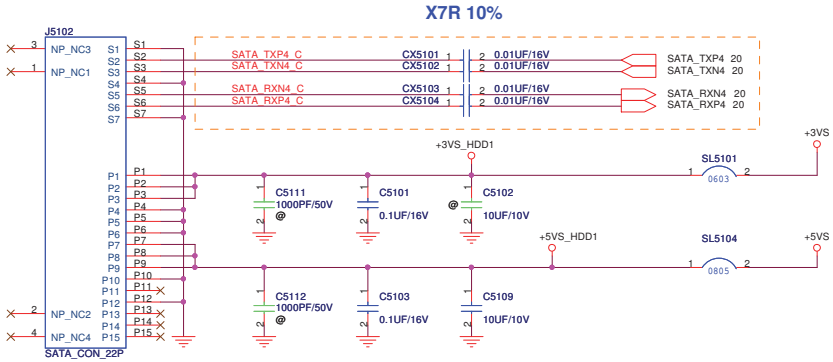
http://laptop-motherboard-schematic.blogspot.com/

ODD



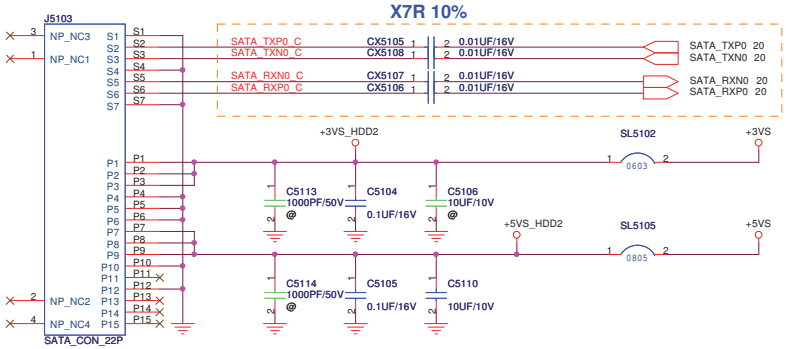
12G151010136

HDD (2nd) Right side



12G15112022J

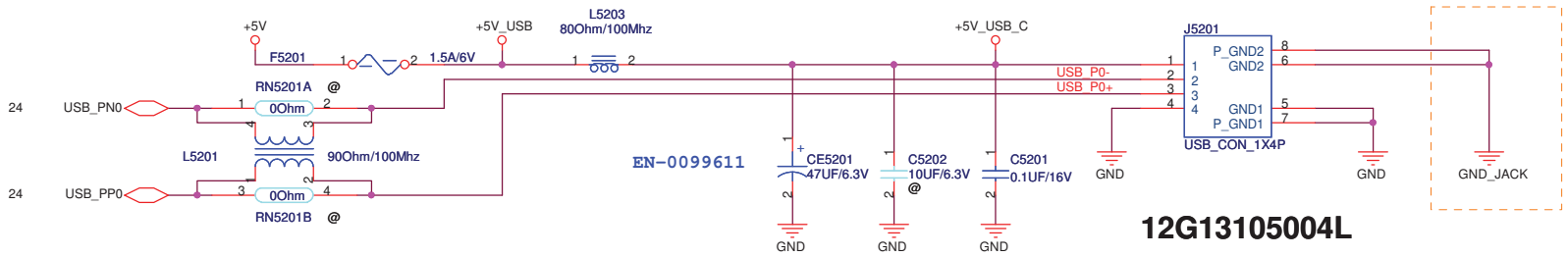
HDD (1st) Left side

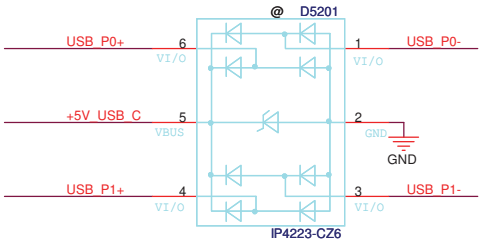


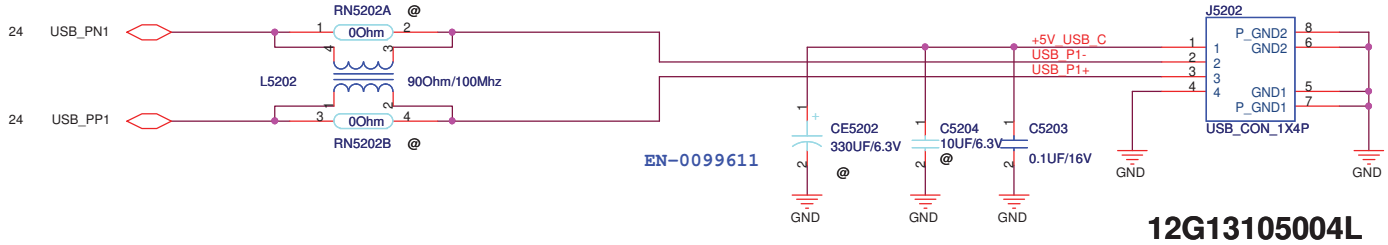
12G15112022J

ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD		
	Engineer: Jerry Mou		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, December 11, 2009	Sheet 51 of 100		

http://laptop-motherboard-schematic.blogspot.com/



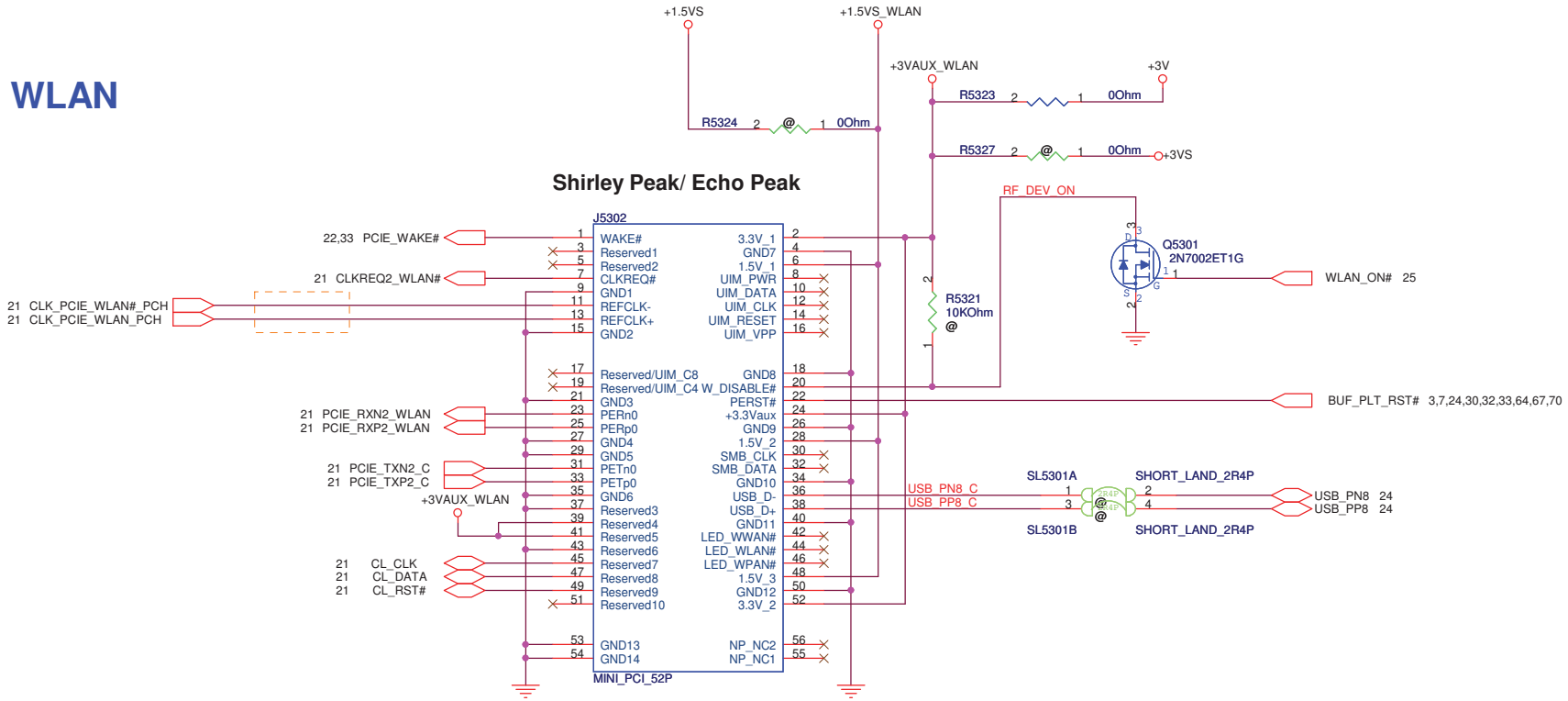




ASUS	Title : USB Port	
ASUSTeK COMPUTER INC. NB4	Engineer: Jerry Mou	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 52 of 100	

http://laptop-motherboard-schematic.blogspot.com/

WLAN

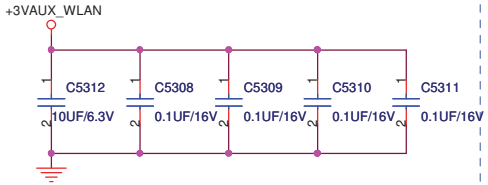


12G03011052N

WLAN +3VAUX bypass capacitor:

Place 0.1UF near pin 2,24,52,39 41.

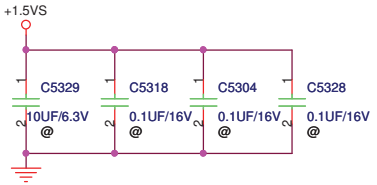
Place 10UF near +3VAUX_WLAN source side.



WLAN +1.5VS bypass capacitor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.



WLAN nuts:

Minicard spec R1.2:

Full size card= 2pcs.

Half size card= 2pcs.

13G021043011 **13G021043011**

2ND : 13G021085000

ASUSTeK COMPUTER INC. NB6	Title : MINICARD(WLAN)		
	Engineer: Jerry Mou		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, December 11, 2009	Sheet 53 of 100		

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ASUSTeK COMPUTER INC. NB4	Title : BAR_****	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
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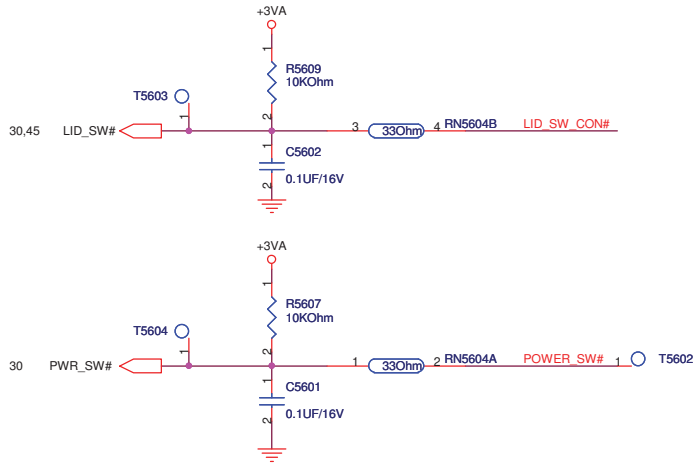
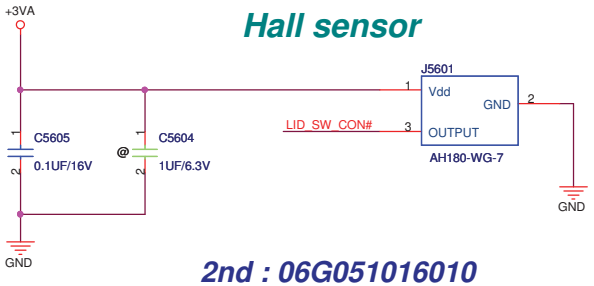
Main Board

ASUSTeK COMPUTER INC. NB4	Title : SIO_****	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
Date: Friday, December 11, 2009	Sheet 55 of 100	

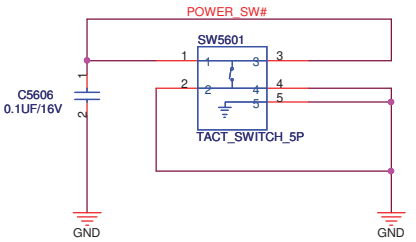
http://laptop-motherboard-schematic.blogspot.com/



Hall sensor



POWER BUTTON

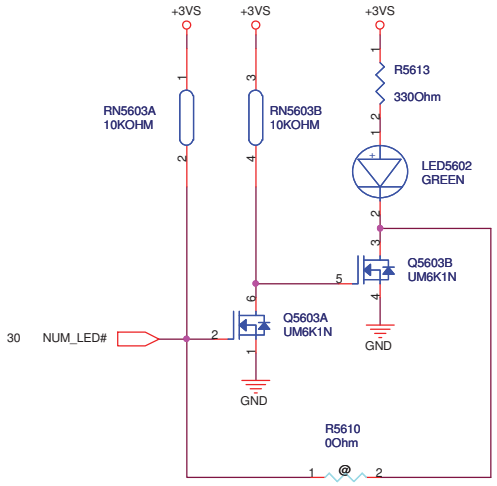


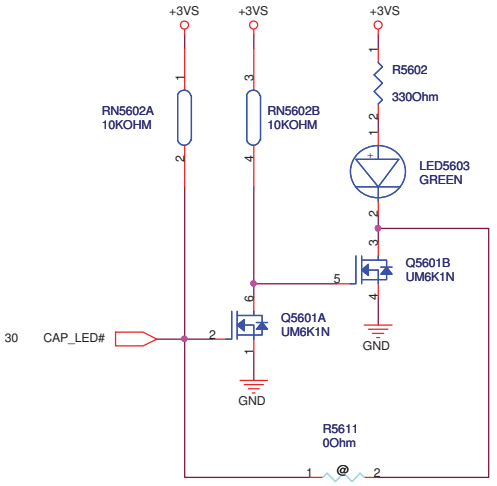
2nd : 06G051016010

(3rd : 06G036022010)

2nd : 07G015200351

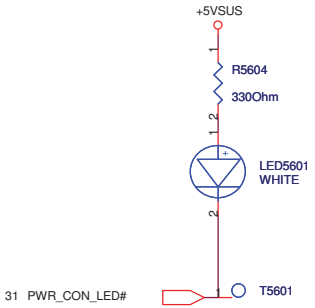
(3rd : 07G015500051)





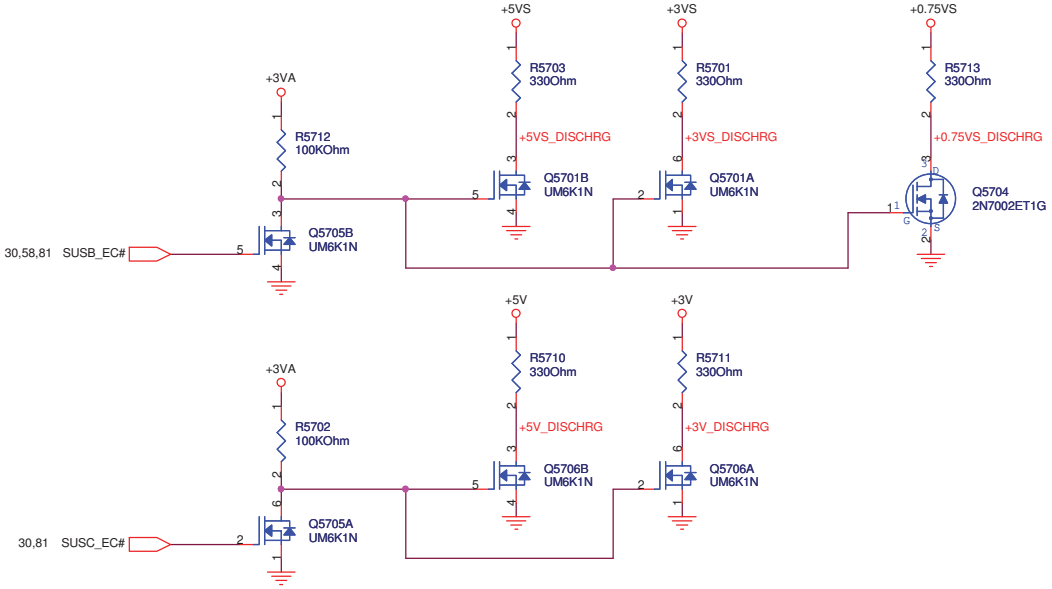
2nd : 07G01570130A

(3rd : 07G015L0042A)



ASUS	Title : LED_Indicator	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
Date: Friday, December 11, 2009	Sheet 56 of 100	

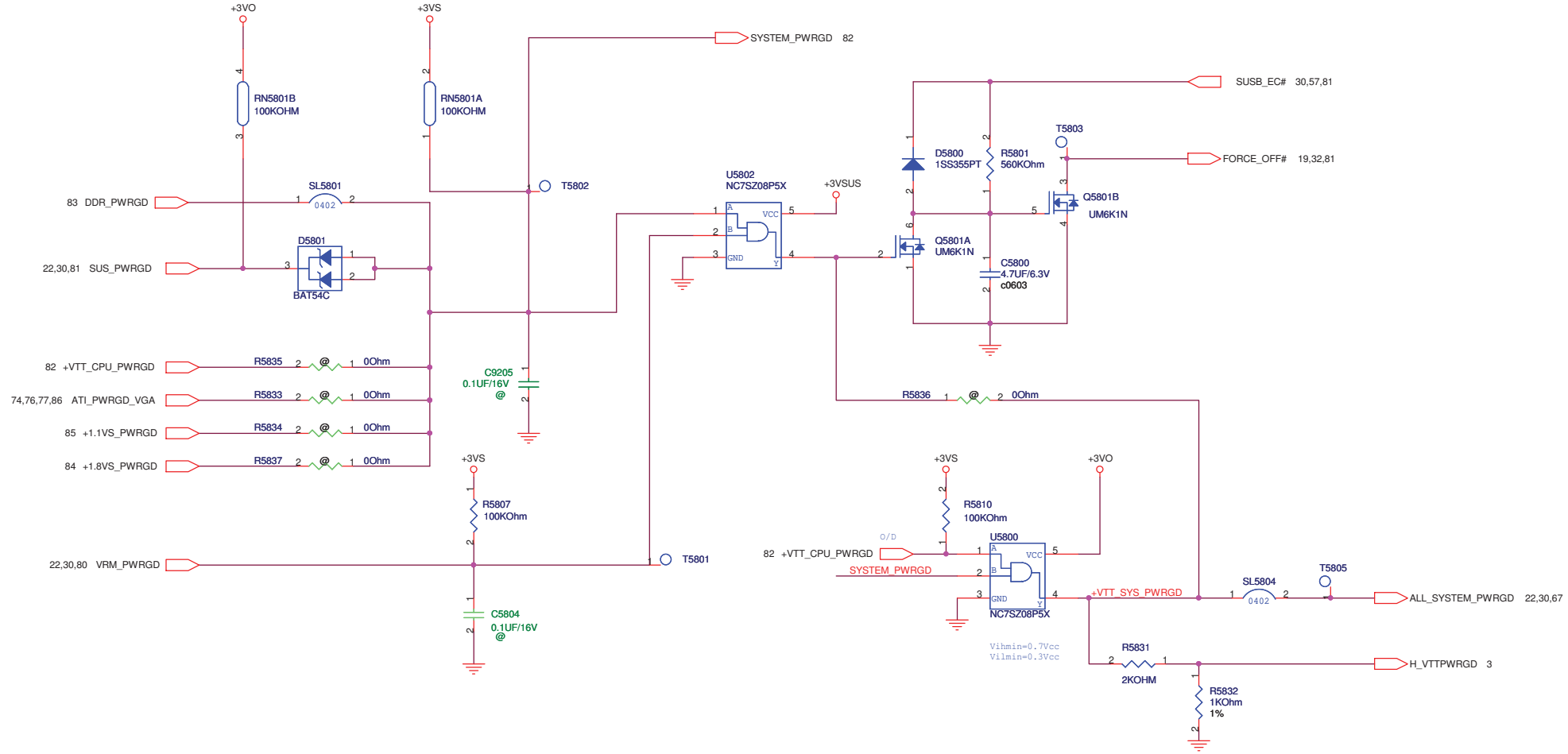
http://laptop-motherboard-schematic.blogspot.com/



ASUS	Title : DSG_Discharge	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
Date: Friday, December 11, 2009	Sheet 57 of 100	

http://laptop-motherboard-schematic.blogspot.com/

POWER GOOD DETECTER



ASUS	Title : PCI_****	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
Date: Friday, December 11, 2009	Sheet 58 of 100	

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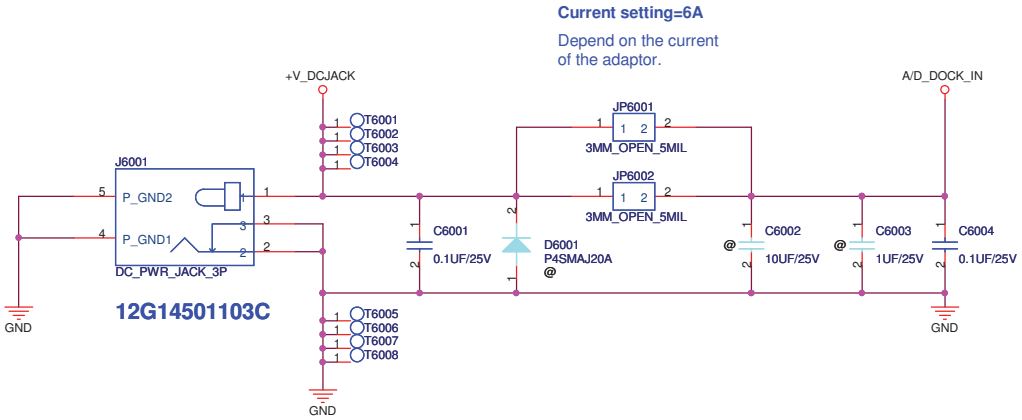
Main Board

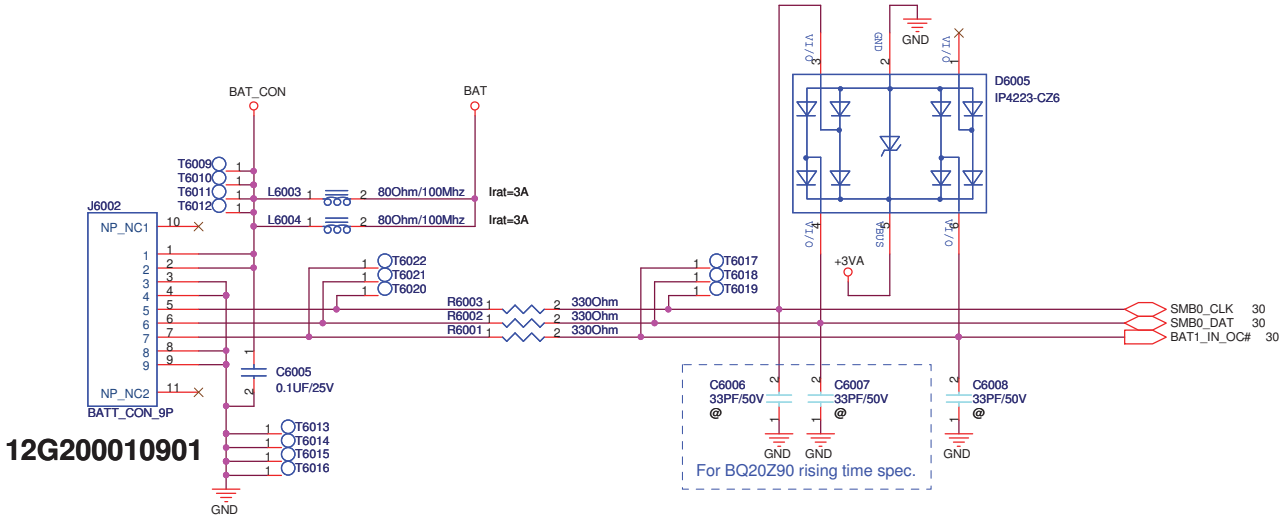
ASUSTeK COMPUTER INC. NB4	Title : DJ_ ****	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
Date: Friday, December 11, 2009	Sheet 59 of 100	

http://laptop-motherboard-schematic.blogspot.com/

DC Jack



Battery Connector



ASUS	Title : DC_DC & BAT Conn.	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
Date: Friday, December 11, 2009	Sheet 60 of 100	

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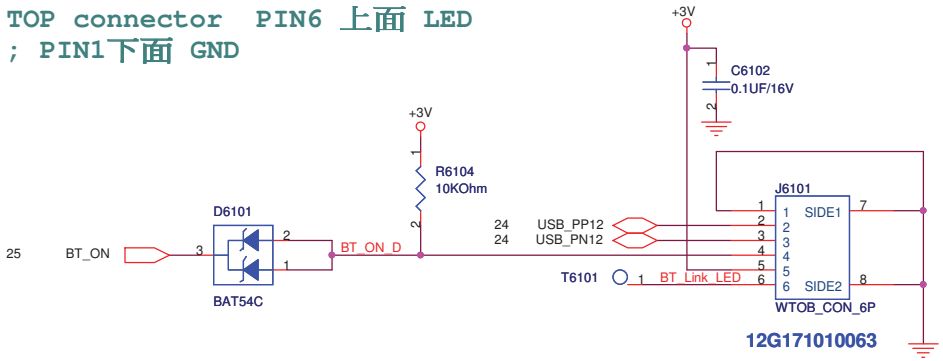
BLUETOOTH

TOP connector PIN6 上面 LED
; PIN1下面 GND



ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 61 of 100	

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Main Board

ASUSTeK COMPUTER INC. NB4	Title : TPM_****	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
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Main Board

ASUSTeK COMPUTER INC. NB4	Title : FP_FP Conn	
	Engineer: Ryan_Wang	
Size C	Project Name K72Jr	Rev 1.0
Date: Friday, December 11, 2009	Sheet 63 of 100	

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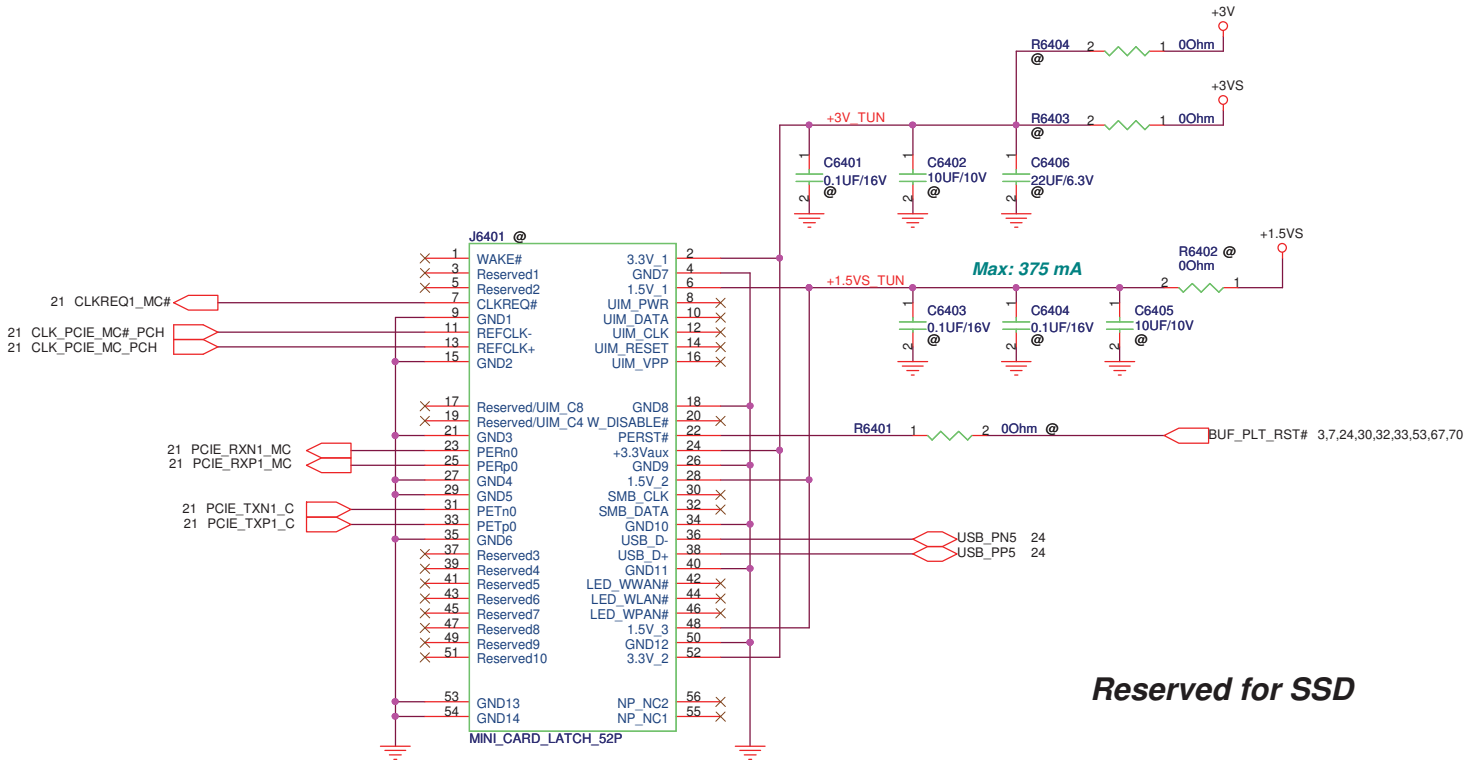
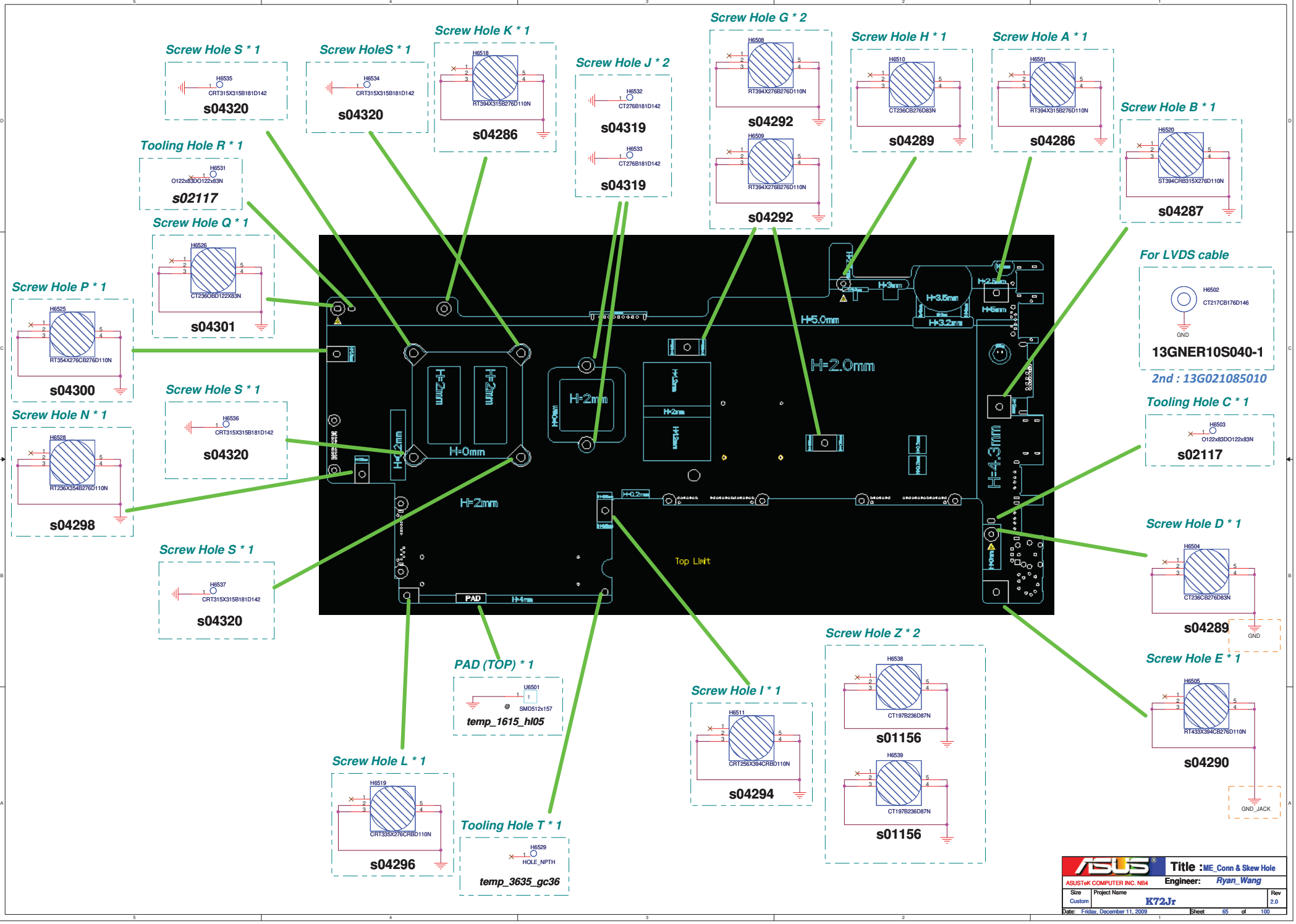


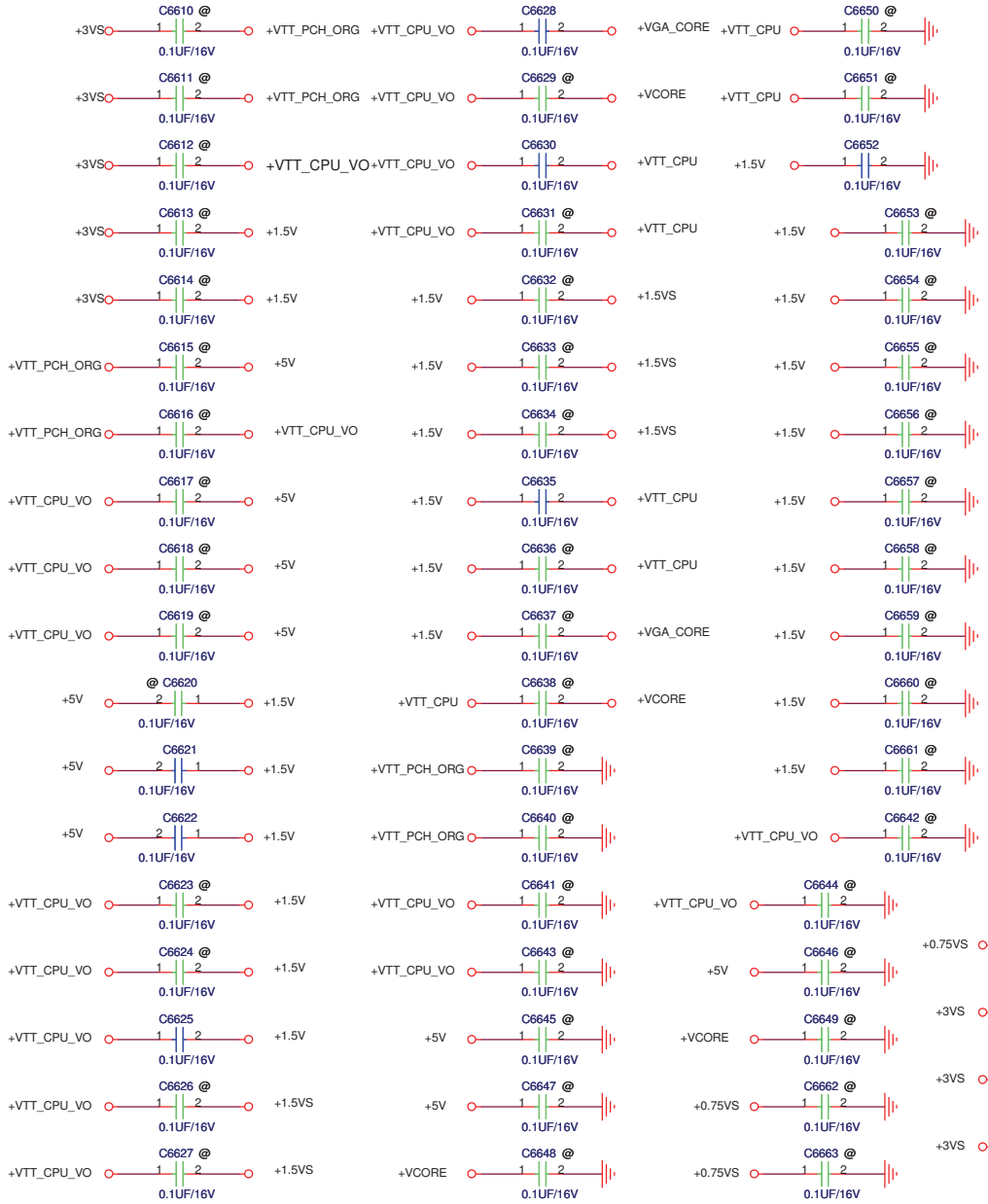
ASUS	Title :		
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang		
Size Custom	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009	Sheet 64 of 100		

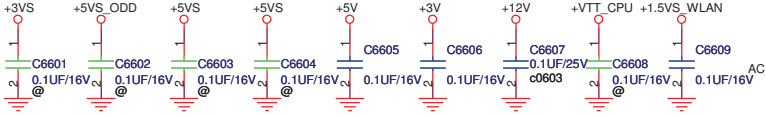
http://laptop-motherboard-schematic.blogspot.com/

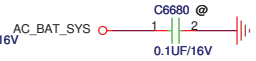


http://laptop-motherboard-schematic.blogspot.com/

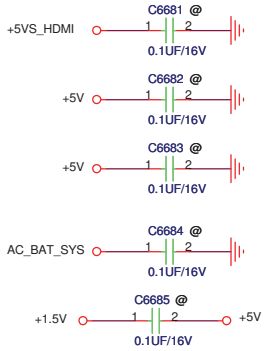
Main Board

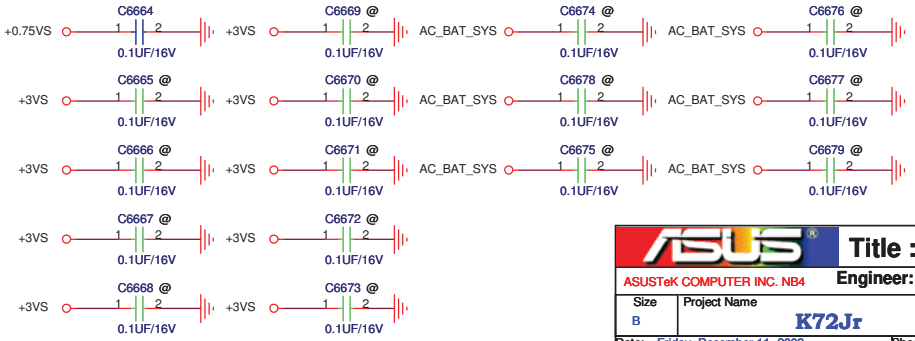






1.在(10980、4170)附近，預留+3VS對GND之0402電容
2.在(2050、2040)附近，預留+5VS_ODD對GND 之0402電容
3.在(2020、2355)附近，預留+5VS對GND之0402電容
4.在(760、5980)附近，預留+5VS對GND之0402電容
5.在(645、3670)附近，預留+5V對GND之0402電容
6.在(655、3930)附近，預留+3V對GND之0402電容
7.在(660、4025)附近，預留+12V對GND之0402電容
8.在(1875、5145)附近，預留+VTT_CPU對GND之0402電容
9.在(8170、4415)附近，預留+1.5VS_WLAN對GND之0402電容
10.ACZ_BCLK_AUD 對 GND，在(11270、3545)預留10pF電容
11.+3VS對+VTT_PCH_ORG，在(10415、5140)、(8595、5175)處預留0402 0.1uF電容
12.+3VS對+VTT_CPU_VO，在(8255、4785)處預留0402 0.1uF電容
13.+3VS對+1.5V，在(8075、4620)、(7765、3245)處預留0402 0.1uF電容
14.+VTT_PCH_ORG對+5V，在(9965、5945)處預留0402 0.1uF電容
15.+VTT_PCH_ORG對+VTT_CPU_VO，在(8445、5760)處預留0402 0.1uF電容
16.+VTT_CPU_VO對+5V，在(7745、5940)、(4985、5945)、(1105、5520)處預留電0402 0.1uF容
17.+5V對+1.5V，在(1480、3920)、(1490、3650)、(1435、3330)處預留0402 0.1uF電容
18.+VTT_CPU_VO對+1.5V，在(7570、5495)、(7840、5380)、(3855、4580)處預留0402 0.1uF電容
19.+VTT_CPU_VO對+1.5VS，在(7090、5535)、(5765、5485)處預留0402 0.1uF電容
20.+VTT_CPU_VO對+VGA_CORE，在(4250、5365)處預留0402 0.1uF電容
21.+VTT_CPU_VO對+VCORE，在(2705、5680)處預留電0402 0.1uF容
22.+VTT_CPU_VO對+VTT_CPU，在(2020、5210)、(1435、5060)處預留0402 0.1uF電容
23.+1.5V對+1.5VS，在(7140、5265)、(7045、4495)、(5555、3705)處預留0402 0.1uF電容
24.+1.5V對+VTT_CPU，在(1735、4210)、(2870、4255)處預留0402 0.1uF電容
25.+1.5V對+VGA_CORE，在(4760、4240)處預留0402 0.1uF電容
26.+VTT_CPU對+VCORE，在(2900、4855)處預留0402 0.1uF電容
27.+VTT_PCH_ORG對GND，在(10195、5215)、(9340、5705)處預留電容
28.+VTT_CPU_VO對GND，在(8250、4895)、(1380、4800)、(3730、4480)、(5860、5740)處預留0402 0.1uF電容
29.+5V對GND，在(9120、6280)、(5795、5990)、(815、6065)處預留0402 0.1uF電容
30.+VCORE對GND，在(3080、5515)、(2170、6130)處預留0402 0.1uF電容
31.+VTT_CPU對GND，在(2855、4370)、(3195、4675)處預留0402 0.1uF電容
32.+1.5V對GND，在(2630、3935)、(1975、2675)、(1995、1830)、(5025、2055)、(4355、3930)、(5480、3215)、(6785、3080)、(7275、3765)、(7885、4435)、(7325、5370)處預留0402 0.1uF電容
33.+0.75VS對GND，在(2240、2160)、(2190、1865)、(2285、1355)處預留0402 0.1uF電容
34.+3VS對GND，在(11580、6925)、(10970、5800)、(11890、3700)、(11845、2860)、(10535、4655)、(10175、3090)、(9210、4205)、(8690、4755)、(6935、3050)處預留0402 0.1uF電容
35.AC_BAT_SYS對GND，在(11090、6810)、(7715、6300)、(11965、5415)、(920、6010)、(1075、3230)、(9410、3380)、(10880、4230)處預留0402 0.1uF電容
36.+5VS_HDMI對GND，(12210、3790)預留0402 0.1uF電容
37. +5V對GND，(11040、5595)、(11480、6860)預留0402 0.1uF電容
38.+1.5V對+5V，(915、3445)預留0402 0.1uF電容
39.AC_BAT_SYS對GND，(1075、5230)預留0402 0.1uF電容





ASUS	Title :	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
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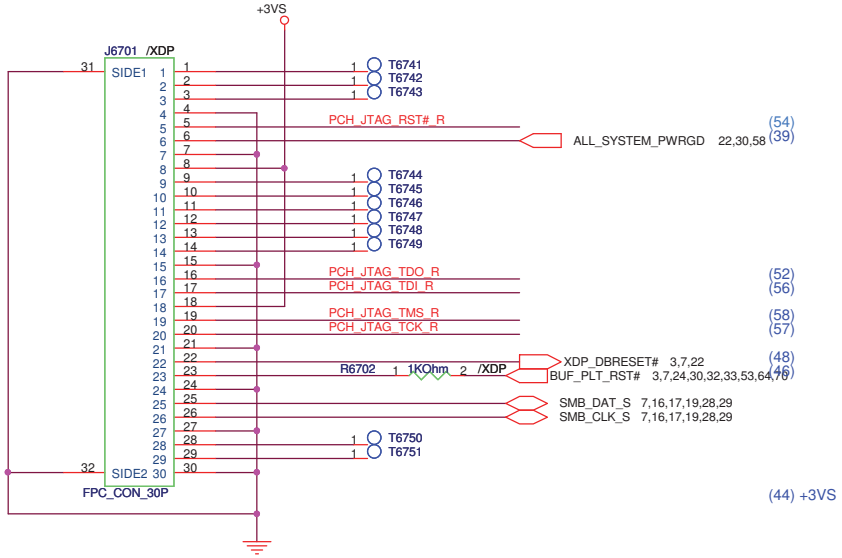
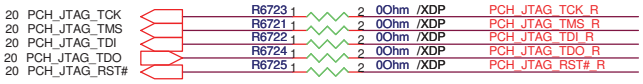
PCH XDP





ASUSTeK COMPUTER INC. NB4	Title : PCH_XDP	
	Engineer: Ryan_Wang	
Size: B	Project Name: K72Jr	Rev: 2.0
Date: Friday, December 11, 2009	Sheet 67 of 100	

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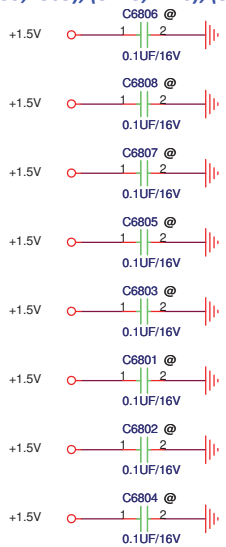
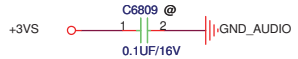
2009/8/25

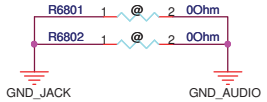
1.5V對GND, (1975,4025), (3250,4075), (3325,2310), (3870,2300), (3445,1720), (3735,1805), (3225,1420), (3635,1500)預留0402電容



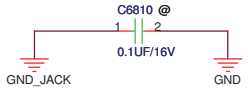
INT_MIC 跨 +3VS & GND_Audio 在in2切割，預留+3VS對GND_AUDIO 電容



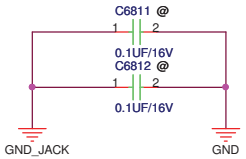
GND_Jack對GND_AUDIO留0歐姆電阻: (11990, 2240), (11895, 1695)



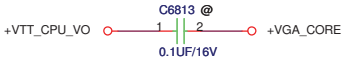
GND_Jack對GND: (12015, 2405)預留電容



GND_audio對GND: (11655, 2495), (11655, 2200)預留電容



+VTT_CPU_VO對+VGA_Core: (5310, 5430)預留電容



+5V對+VTT_CPU_VO:(2565, 5990)預留電容

ASUS	Title : OTH_LCM	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0
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ASUS	Title : OTH_GAME-LED*****	
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang	
Size: C	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 69 of 100	

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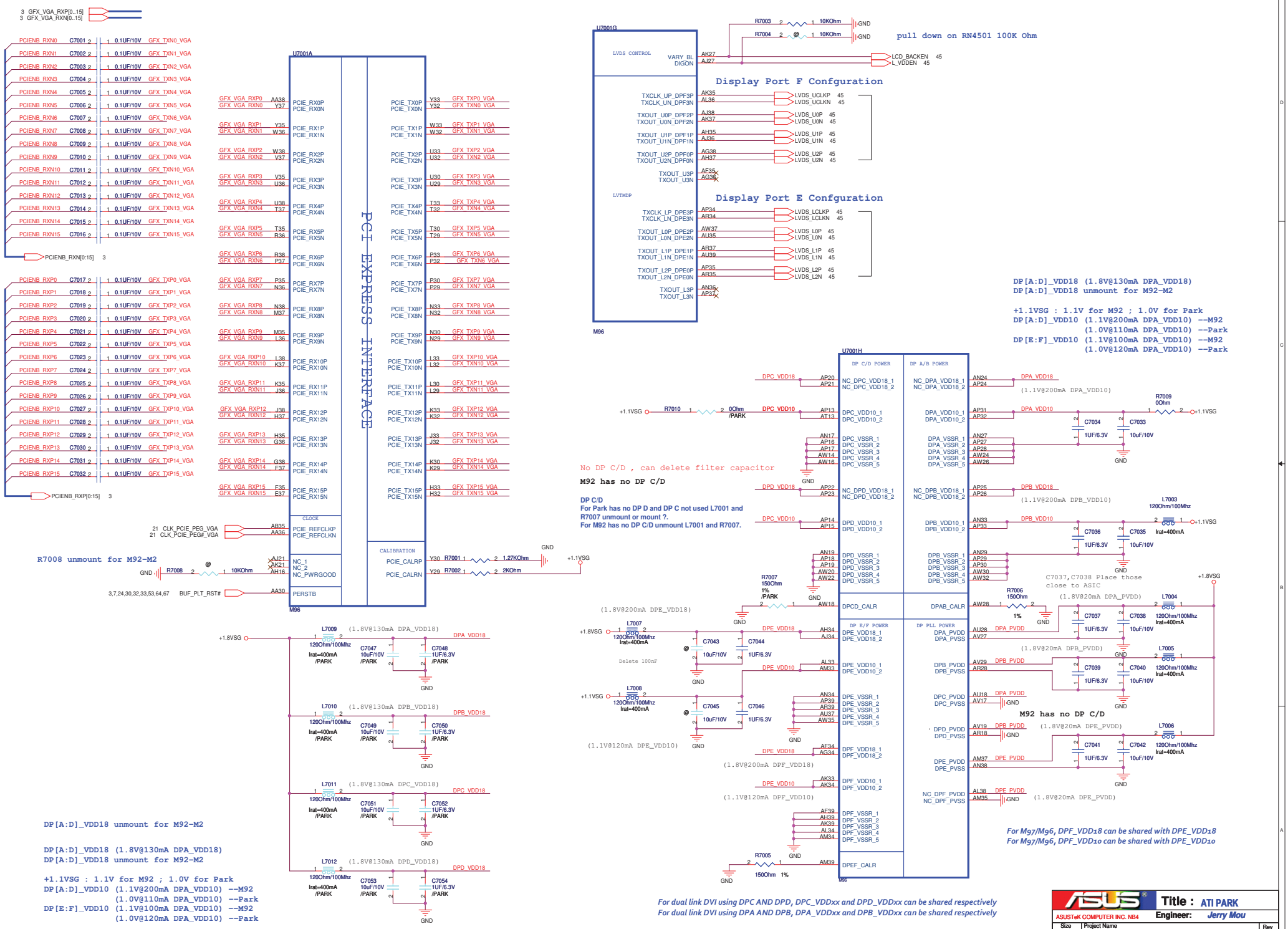

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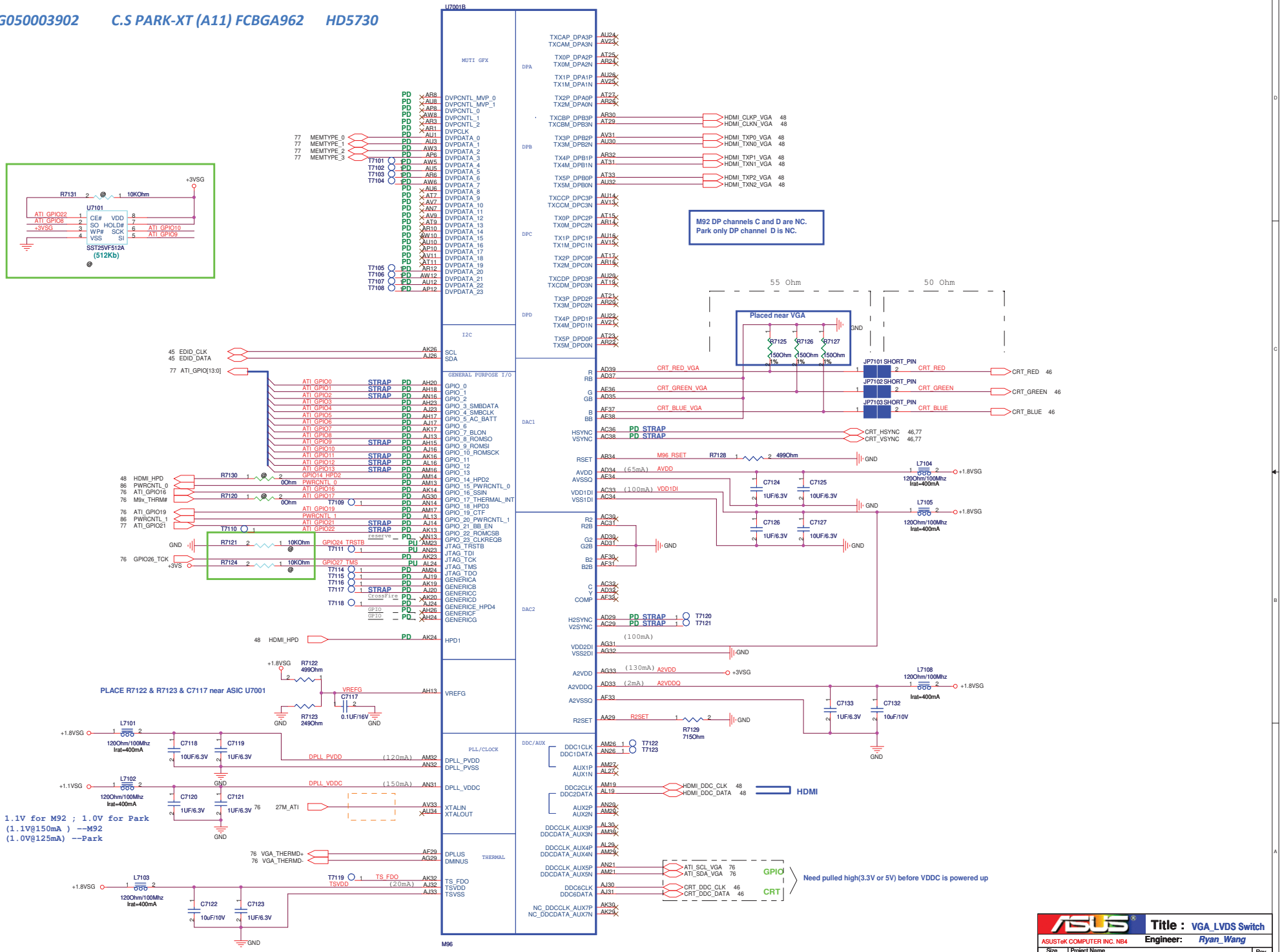
02G050003902 C.S PARK-XT (A11) FCBGA962 HD5730



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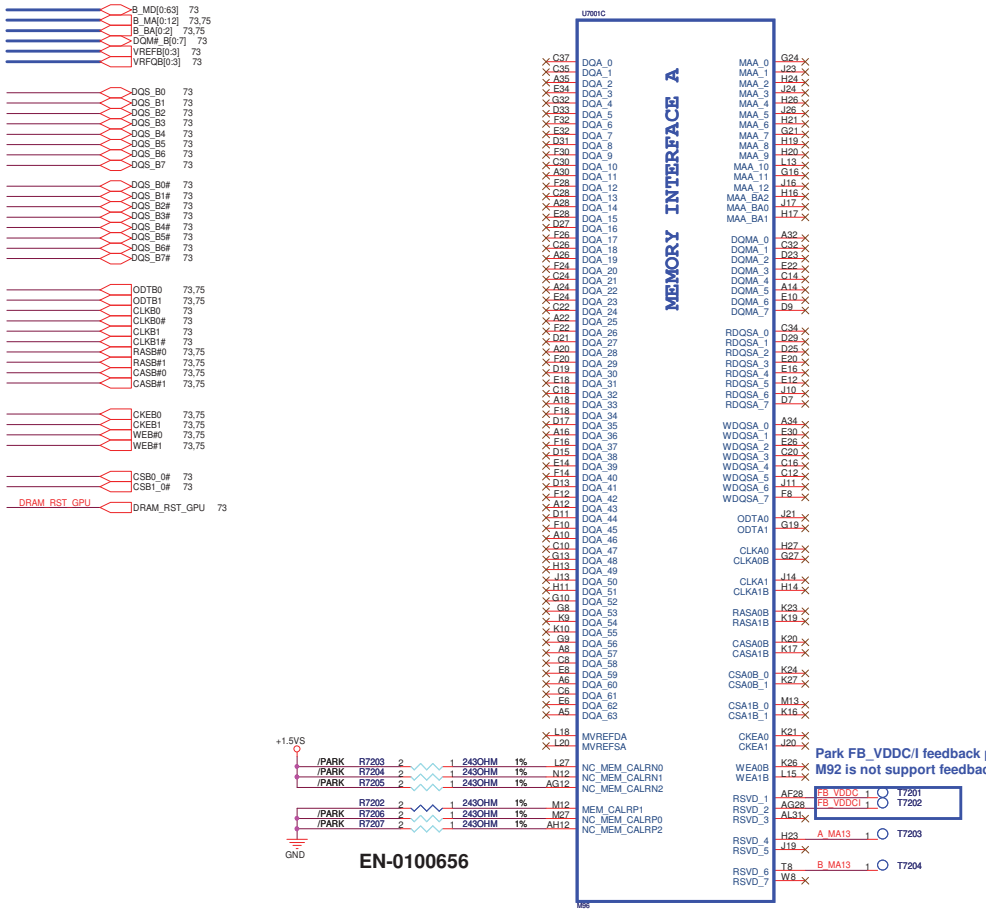
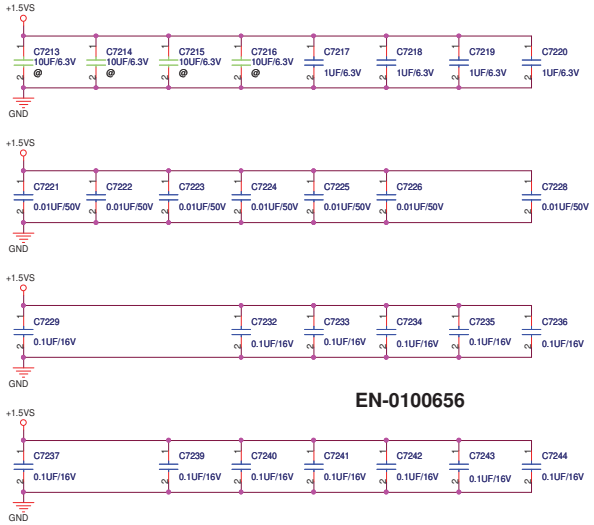
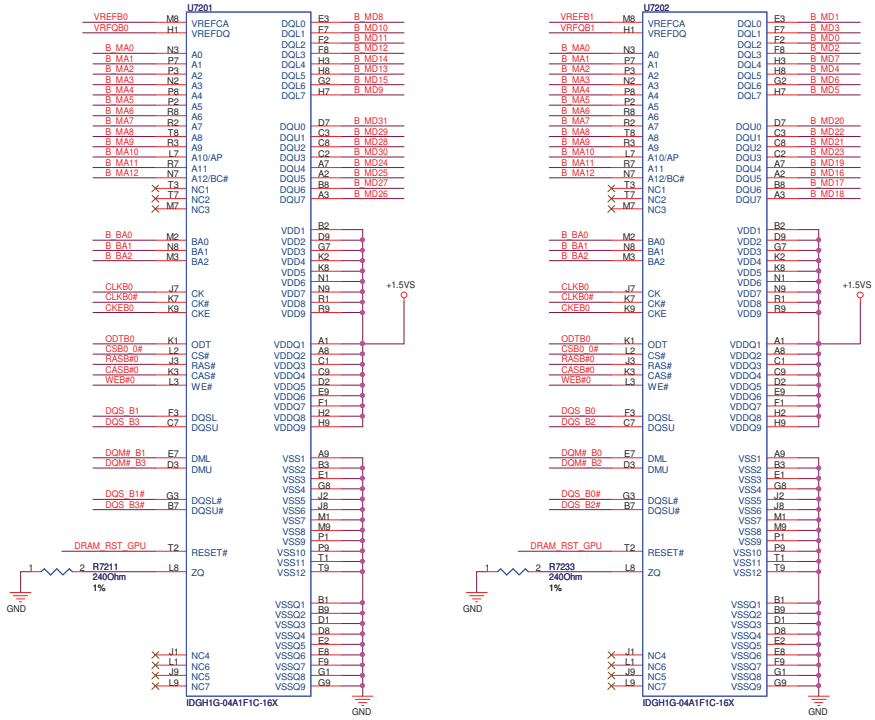
Channel B: Dual 1GB Rank DDR3 (Rank0)

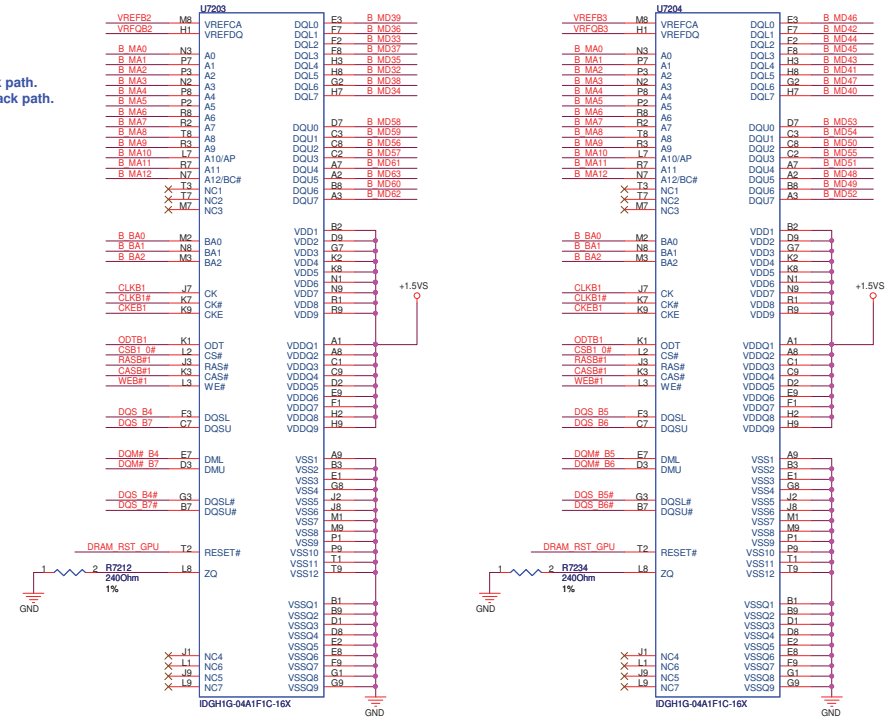


EN-0100656



EN-0100656





03G151638421 DDR3 64M*16-1.2 FBGA-96 HYNIX/H5TQ1G63BFR-12C

ASUS	Title : VRAM RANK0		
ASUSTeK COMPUTER INC. NB4	Engineer: Jerry Mou		
Size C	Project Name K72Jr		Rev 2.0
Date: Friday, January 22, 2010	Sheet 72 of 100		

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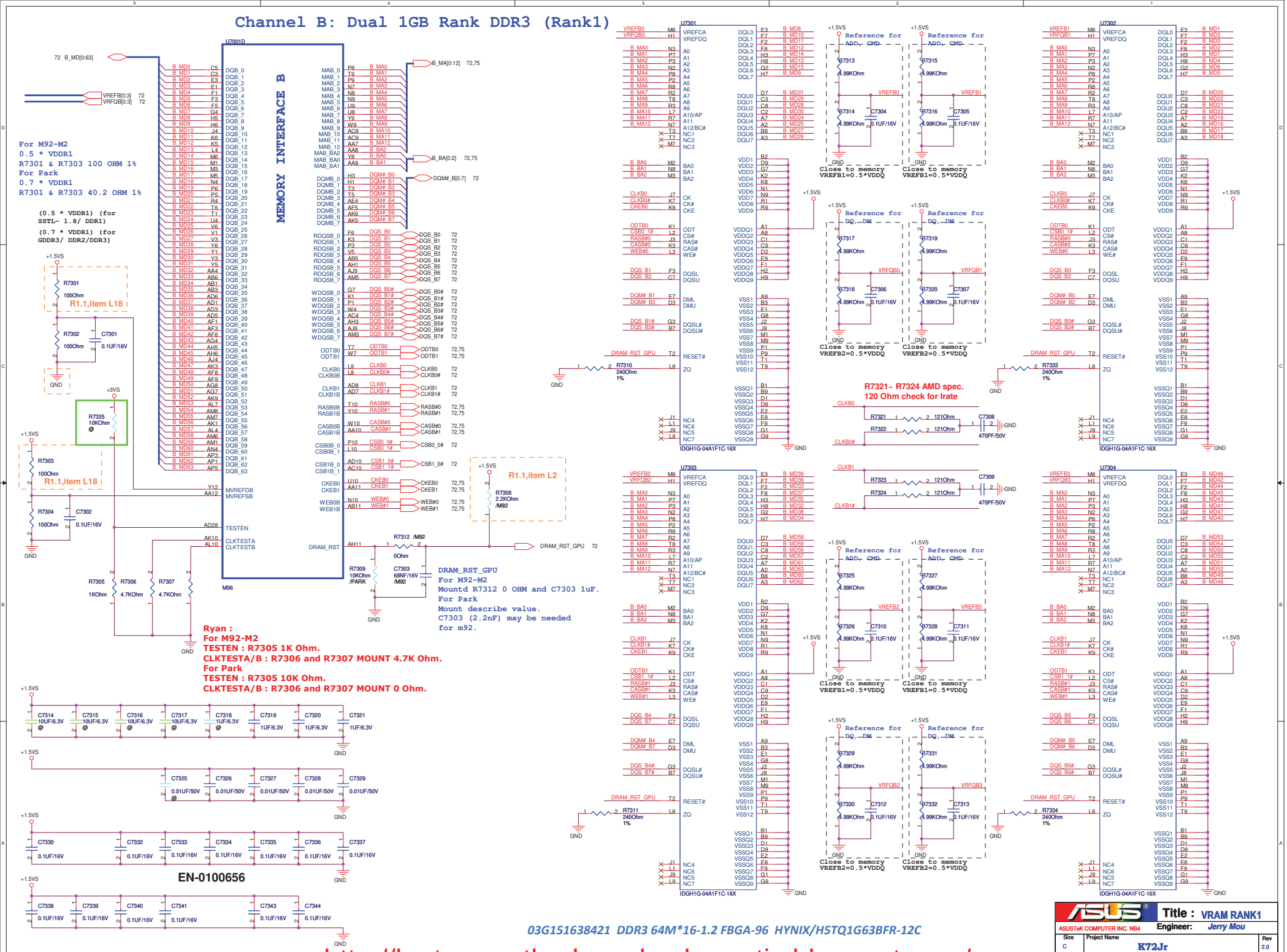
Channel B: Dual 1GB Rank DDR3 (Rank1)



03G151638421 DDR3 64M*16-1.2 FBGA-96 HYNIX/H5TQ1G63BFR-12C

ASUS / ASUSTeK COMPUTER INC. NB4	Title : VRAM RANK1		
	Engineer: Jerry Mou		
Size C	Project Name K72Jr		Rev 2.0
Date: Friday, January 22, 2010	Sheet 73 of 100		

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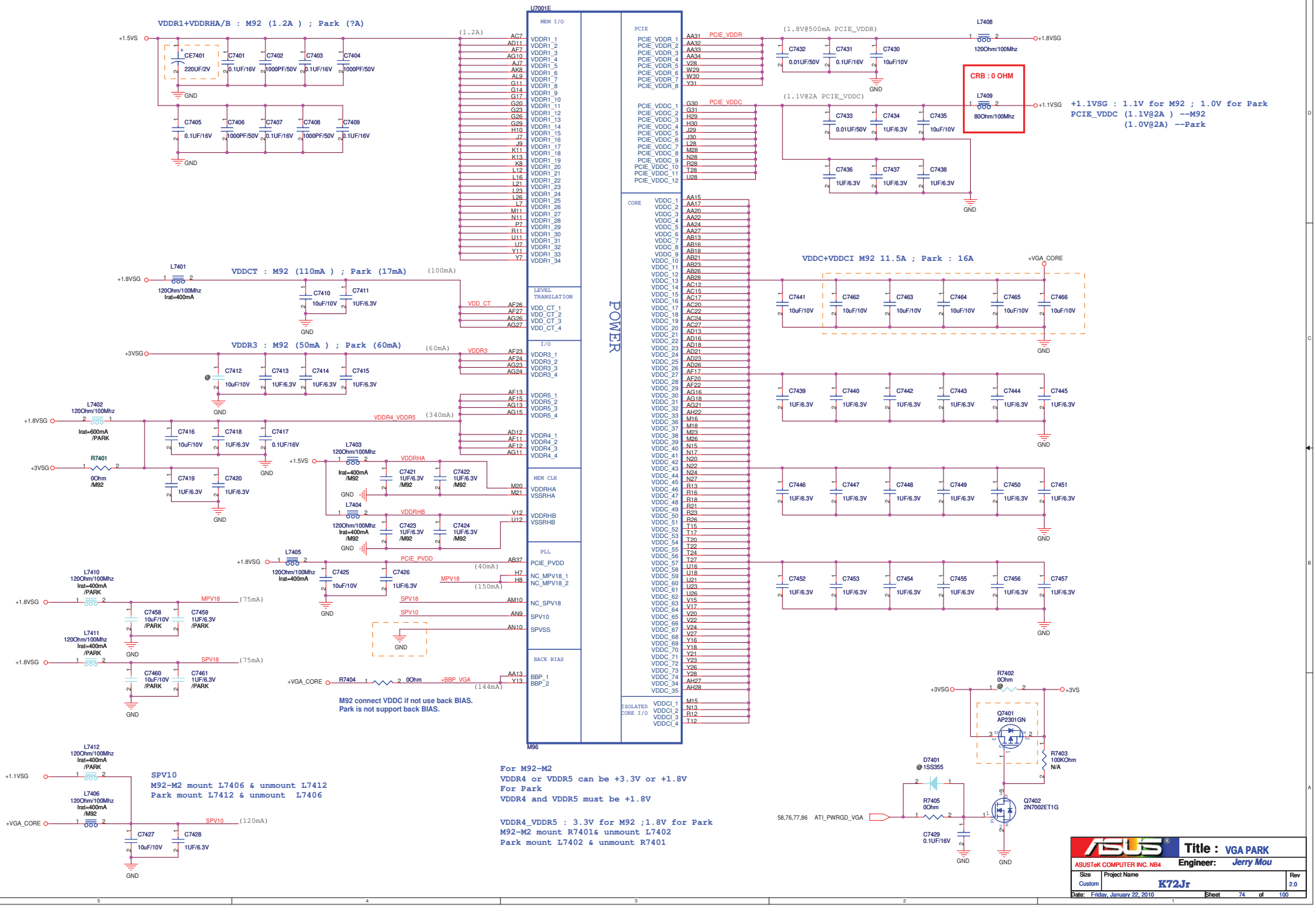
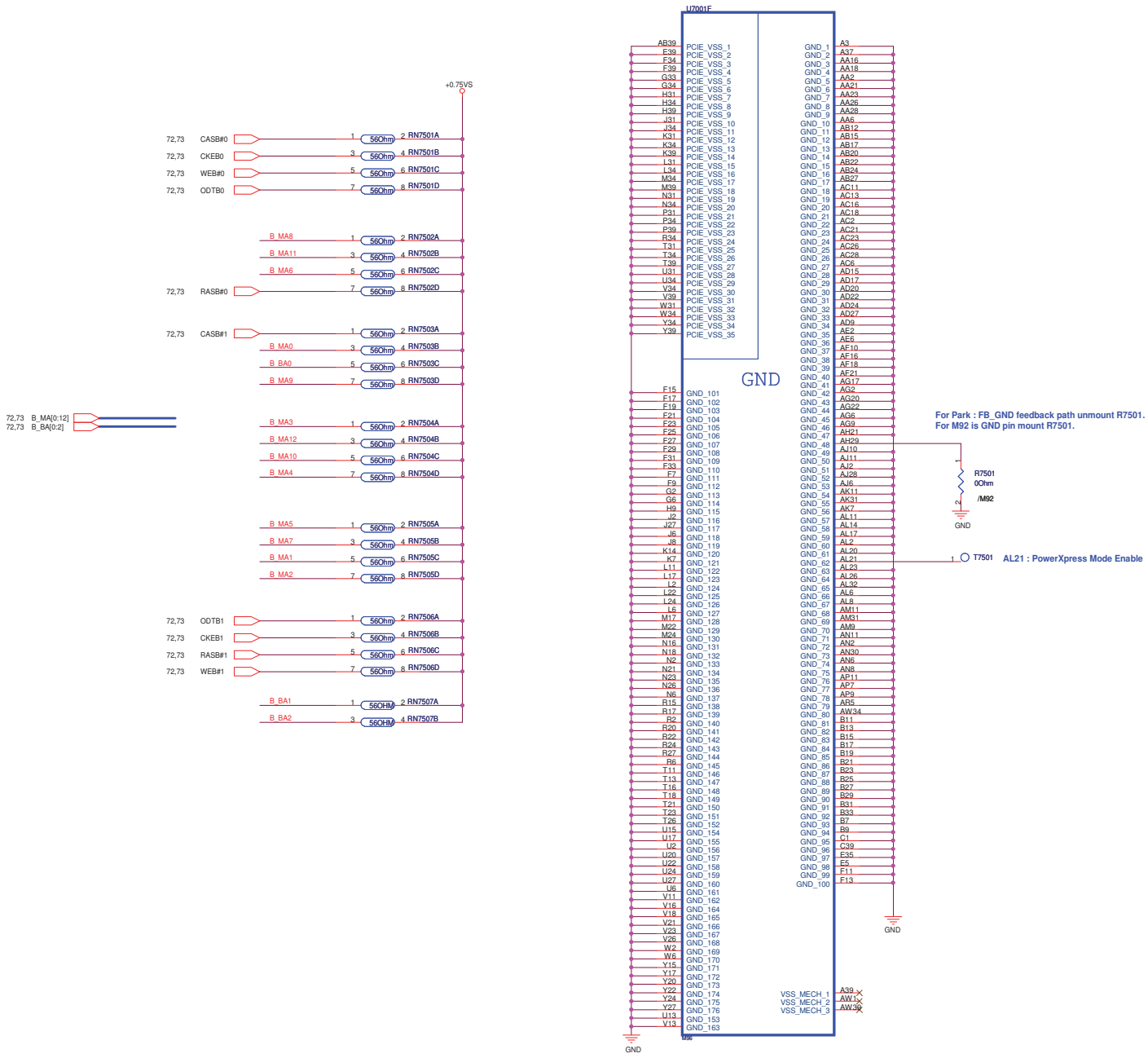


http://laptop-motherboard-schematic.blogspot.com/



ASUSTeK COMPUTER INC. NB4	Title : VGA_power		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: K72Jr		Rev: 2.0
Date: Friday, January 22, 2010	Sheet 75 of 100		

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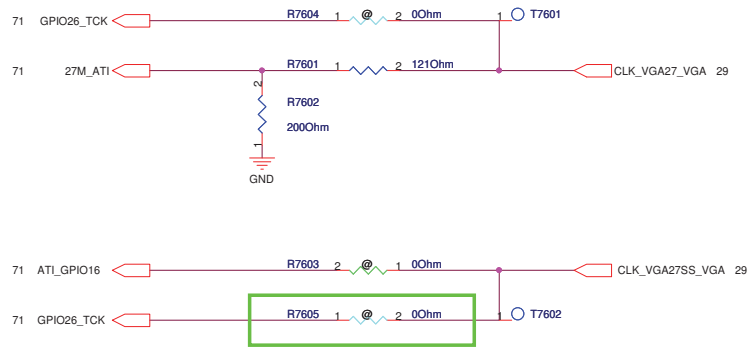
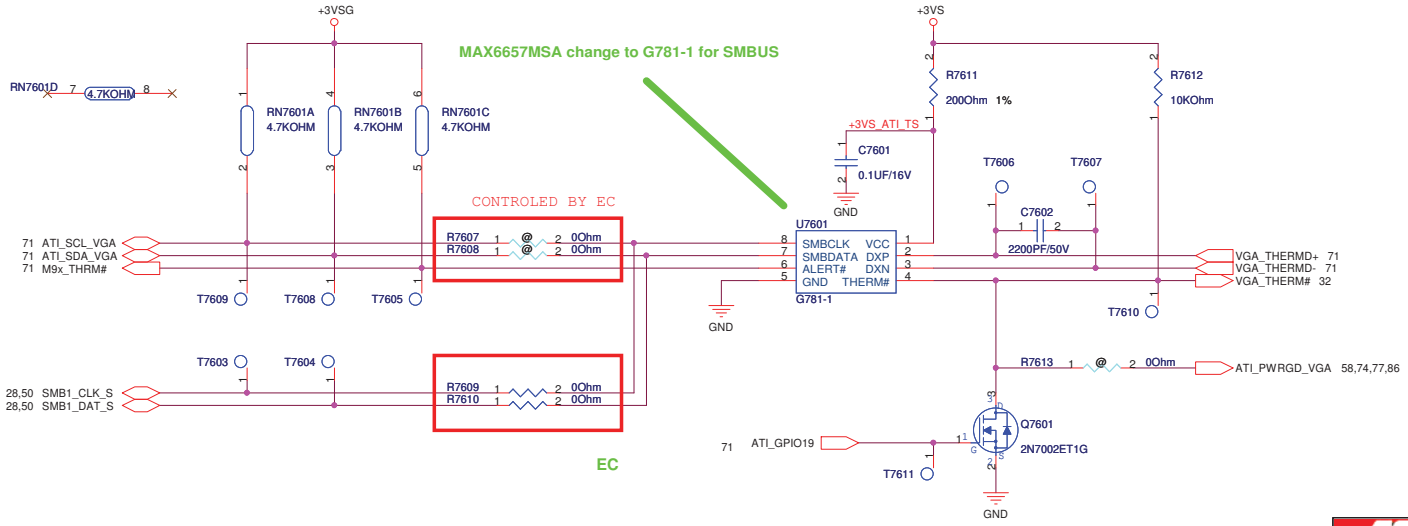
Memory Clock SS (Reserved)

S0 (Spread Percentage Select):
GND: TBD%
VDD: TBD% (default PU)
NC : TBD%



	SMBUS SLAVE ADDRESS
G781	98 (1 0 0 1 1 0 0)
G781-1	9A (1 0 0 1 1 0 1)



ASUS	Title : VGA_****		
ASUSTeK COMPUTER INC. NB4	Engineer: Ryan_Wang		
Size: Custom	Project Name: K72Jr		Rev: 2.0
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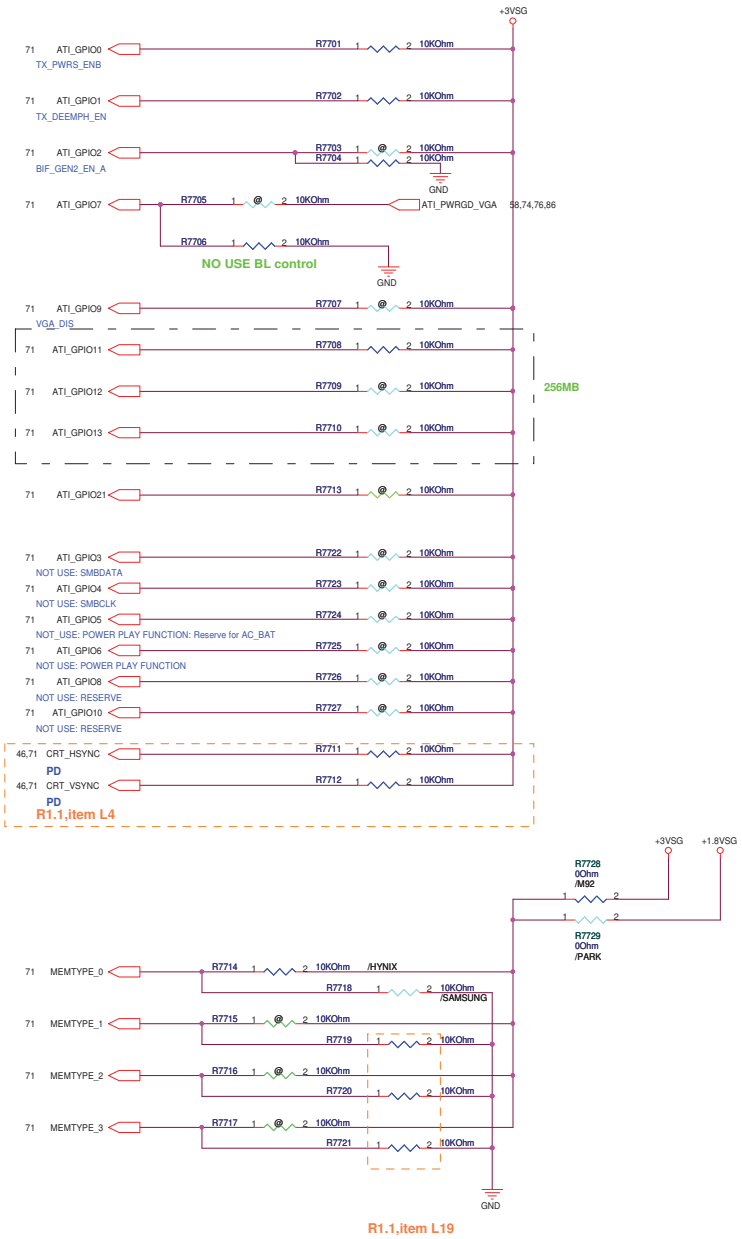
OPTION STRAPS



VDDR4_VDDR5 : 3.3V for M92 ;1.8V for Park
M92-M2 mount R7401& unmount L7402
Park mount L7402 & unmount R7401

M92 Straps

	STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
	VIP_DEVICE_STRAP_EN	V2SYNC	0 - Ignore VIP device straps (DVPDATA_20) 1 - Use VIP device straps (DVPDATA_20)	0 (internal pull-down)
OK	TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing This setting can only be used if the PCIE bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)
OK	TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0 (internal pull-down)
OK	BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
OK	VGA_DIS	GPIO9	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)
OK	ROMIDCFG(2:0)	GPIO(13:11)	If BIOS_ROM_EN=1,then Config[2:0]defines the ROM type. If BIOS_ROM_EN=0,then Config[2:0]deifnes the primary memoru apeture size. 128MB---x000 32MB---Not Support 2GB---Not Support 256MB---x001 512MB--Not Support 4GB---Not Support 64MB---x010 1GB-----Not Support	0000 (internal pull-down)
OK	BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0 (internal pull-down)
OK	AUD[1] AUD[0]	PEG_CRT_HSYNC_VGA PEG_CRT_VSYNC_VGA	AUD[1:0]: 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 10: Audio for DisplayPort only; 11: Audio for both DisplayPort and HDMI.	0 (internal pull-down)
OK OK	Reserved	H2SYNC GPIO_21_BB_EN GENERICC	ATI internal use only . THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET.	0 (internal pull-down)

AUDIO_EN	VIP_3	Enable HD Audio function in the PCI configuration space 0 - Disable HD Audio 1 - Enable HD Audio	0 (internal pull-down)
64BAR_EN_A	VIP_5	Enable 64-bit BARs Most commonly this strap is left at the default (32-bit BARs)	0 (internal pull-down)
MSI_DIS	VIP_1	Disable Message Signaled Interrupt is both a ROM strap and a pin strap. The pin strap is only applicable if a BIOS ROM is not present	0 (internal pull-down)
VIP_DEVICE	VHAD_0	VIP_DEVICE_STRAP_EN is set 0 =>not used VIP Host interface VIP_DEVICE_STRAP_EN is set 1 =>used VIP Host interface	0 (internal pull-down)
DEBUG ACCESS	GPIO4	Debug_access strap 3.3V ---ON 0V-----OFF	0 (internal pull-down)
DEBUG_ I2C_ENABLE	GPIO6	ATI internal use only . Other logic must not affect this signal during RESET Reconnended to 0	0 (internal pull-down)

Dual Rank DDR3 1GB need AMD check pull low or high for following DDR3 VRAM
03G151638020 DDR3 64M*16-1.2 FBGA-96 SAMSUNG/K4W1G1646E-HC12
03G151638421 DDR3 64M*16-1.2 FBGA-96 HYNIX/H5TQ1G63BFR-12C

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR3 Memory Type	Channel Size
Samsung	0000	0	64M*16 (512MB) Dual Rank 512*2 = 1G	B channel dual-link
Hynix	0001	1	64M*16 (512MB) Dual Rank 512*2 = 1G	B channel dual-link

+VGA_CORE	RTop	RBot	PWRCNTL_0	PWRCNTL_1
0.9V	8K	40K	Low	Low
1V	8K	40K || 60.4K	High	Low
1.1V	8K	40K || 30.1K	Low	High
1.2V	8K	40K ||60.4K || 30.1K	High	High

ASUSTeK COMPUTER INC. NB4	Title : VGA_****	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: K72Jr	Rev: 2.0
Date: Friday, January 22, 2010	Sheet 77 of 100	

http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title :	Engineer: Ryan_Wang
Size: C	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 78 of 100	

http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

ASUS	Title :	
ASUSTeK COMPUTER INC. NB	Engineer: Ryan_Wang	
Size: C	Project Name: K72Jr	Rev: 1.0
Date: Friday, December 11, 2009	Sheet 79 of 100	

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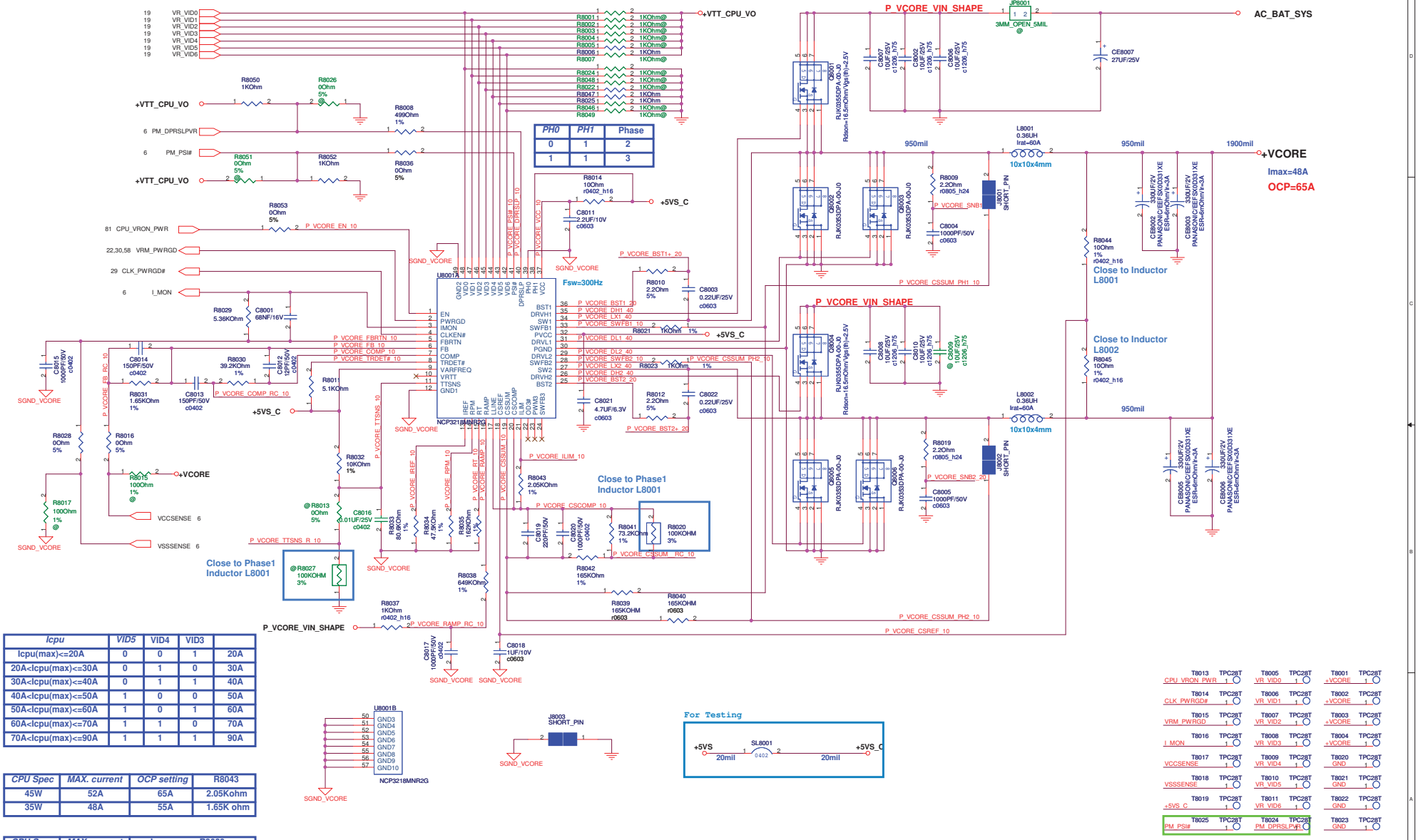
IMVP6.5 CPU VCORE REGULATOR



PH0	PH1	Phase
0	1	2
1	1	3

Icpu	VID5	VID4	VID3	
Icpu(max)<=20A	0	0	1	20A
20A<Icpu(max)<=30A	0	1	0	30A
30A<Icpu(max)<=40A	0	1	1	40A
40A<Icpu(max)<=50A	1	0	0	50A
50A<Icpu(max)<=60A	1	0	1	60A
60A<Icpu(max)<=70A	1	1	0	70A
70A<Icpu(max)<=90A	1	1	1	90A

CPU Spec	MAX. current	OCP setting	R8043
45W	52A	65A	2.05Kohm
35W	48A	55A	1.65K ohm

CPU Spec	MAX. current	I_mon	R8029
45W	50A		5.36Kohm
35W	40A		5.43K ohm

T8013 CPU_VRON_PWR	TPC28T	T8005 VR_VID0	TPC28T	T8001 +VCORE	TPC28T
T8014 CLK_PWRGD#	TPC28T	T8006 VR_VID1	TPC28T	T8002 +VCORE	TPC28T
T8015 VRM_PWRGD	TPC28T	T8007 VR_VID2	TPC28T	T8003 +VCORE	TPC28T
T8016 I_MON	TPC28T	T8008 VR_VID3	TPC28T	T8004 +VCORE	TPC28T
T8017 VCCSENSE	TPC28T	T8009 VR_VID4	TPC28T	T8020 GND	TPC28T
T8018 VSSSENSE	TPC28T	T8010 VR_VID5	TPC28T	T8021 GND	TPC28T
T8019 +5VS_C	TPC28T	T8011 VR_VID6	TPC28T	T8022 GND	TPC28T
T8025 PM_PSI#	TPC28T	T8024 PM_DPRSLPVR	TPC28T	T8023 GND	TPC28T

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : +VCORE

Engineer: CH

Size: Custom | Project Name: K72J | Rev: 1.0

Date: Friday, January 29, 2010 | Sheet 80 of 100

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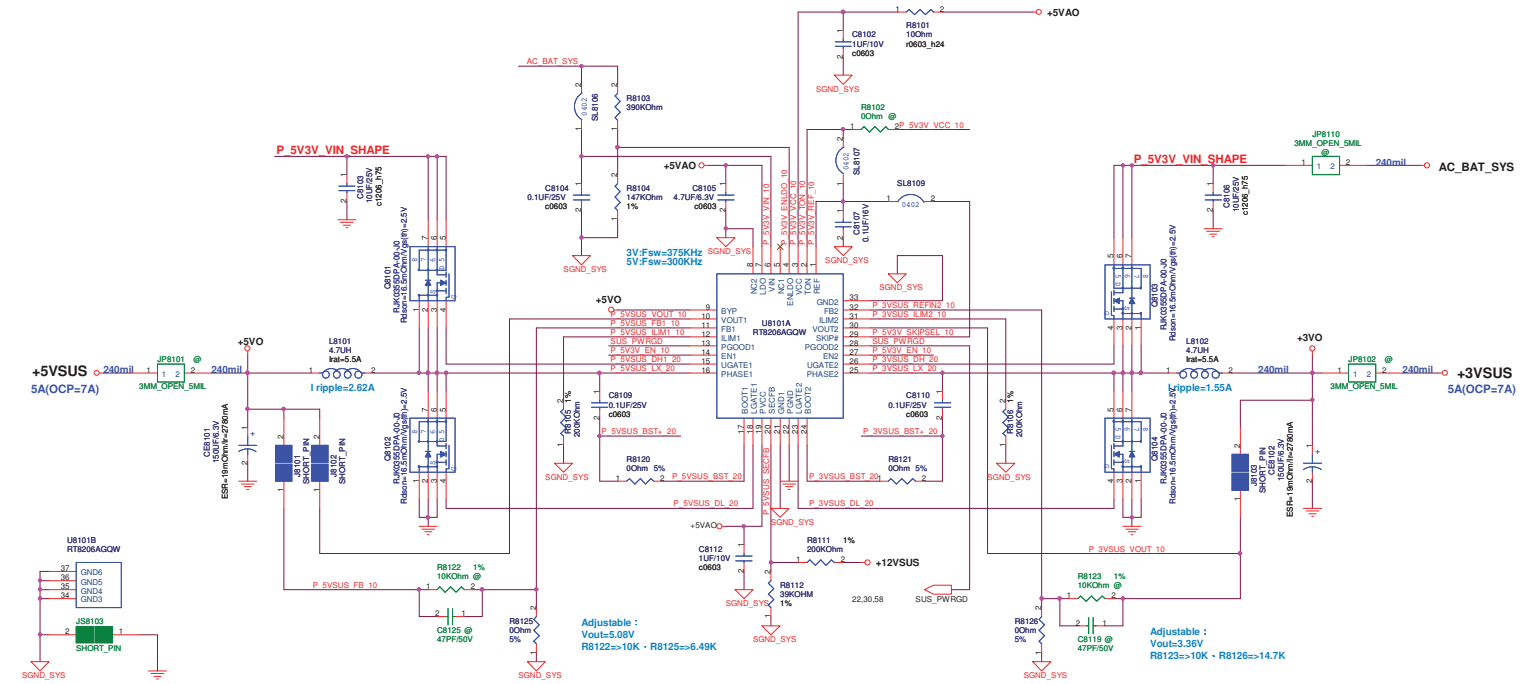


Power stage

+5VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.40A
2. Ripple Current:
   Irip=2.61A
3. Ripple Voltage:
   ESR/1=15mohm
   V=39.15mV
4. Inductor Spec:
   Isat=6.2A
   Idc=5.5A
   DCR=36mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA
   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)
   L-side MOSFET: RJK0355DPA
   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

+3VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=0.93A
2. Ripple Current:
   Irip=1.55A
3. Ripple Voltage:
   ESR/1=15mohm
   V=23.25mV
4. Inductor Spec:
   Isat=6.2A
   Idc=5.5A
   DCR=36mohm

Controller

+5VSUS:

1. Voltage & Current:
   +5VSUS: 5V / 5A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8105=200 Kohm
   Iocp=Rocp/Rds(on)*1e6
   Iocp=7.65A
4. Soft start time:
   The Soft Start duration is 2ms
5. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.25 A

+3.VSUS

1. Voltage&Current:
   +3VSUS: 3.3V / 5A
2. Frequency:
   F=375KHZ
3. OCP:
   Set R8106=200KOhm
   Iocp=Rocp/Rds(on)*1e6
   Iocp=7.25A
4. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.165 A

Part Selection

1. MOSFET:

PPAK56
High Side
RJK0355DPA
07G005B14011(HF)
RJK0355DPA
07G005B14010
Low Side
RJK0355DPA
07G005B14011(HF)
RJK0355DPA
07G005B14010

PPAK33
High Side
SI7326DN
07G005A80011(HF)
Low Side
SI7326DN
07G005A80011(HF)

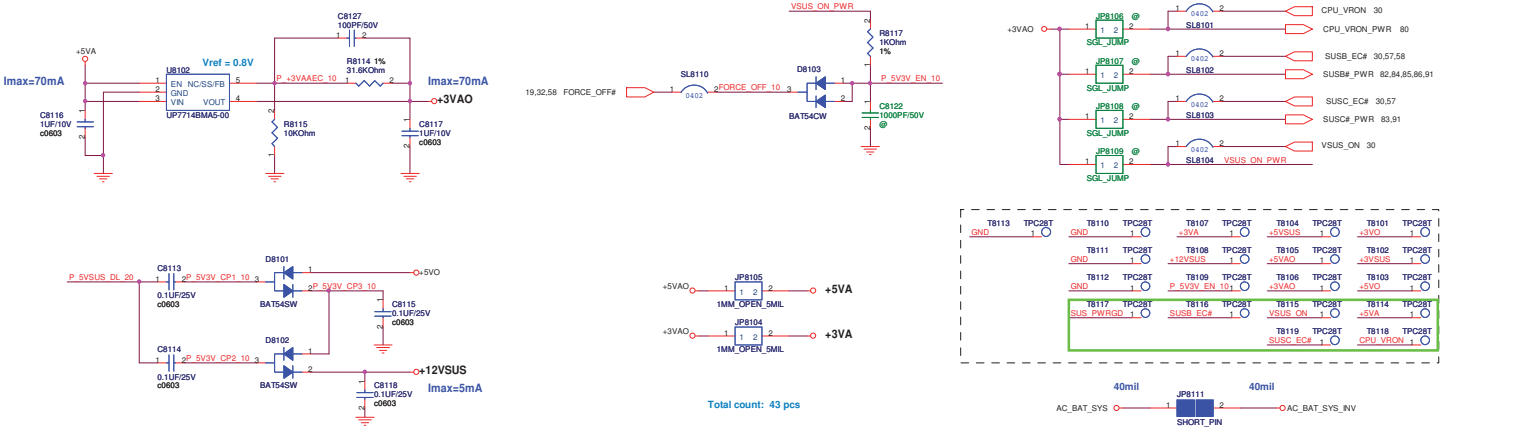
2. Inductor:

Molding063
FDVE0630-H-4R7M=P3
09G02X473037(HF)
PCMC063T-4R7MN
09G02X473032
MPL73-4R7
09G02X473612

Ferrite104
CDRH104REHF-3R8NC
09G02X383402(HF)
B1179BS-H-3R8N
09G02X383403(HF)

3. Output Cap:

7343
EEFCX0J101R
11G08D21075A
EEFCX0J151YR
11G08D415750



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<Variant Name>

Title : POWER_SYSTEM

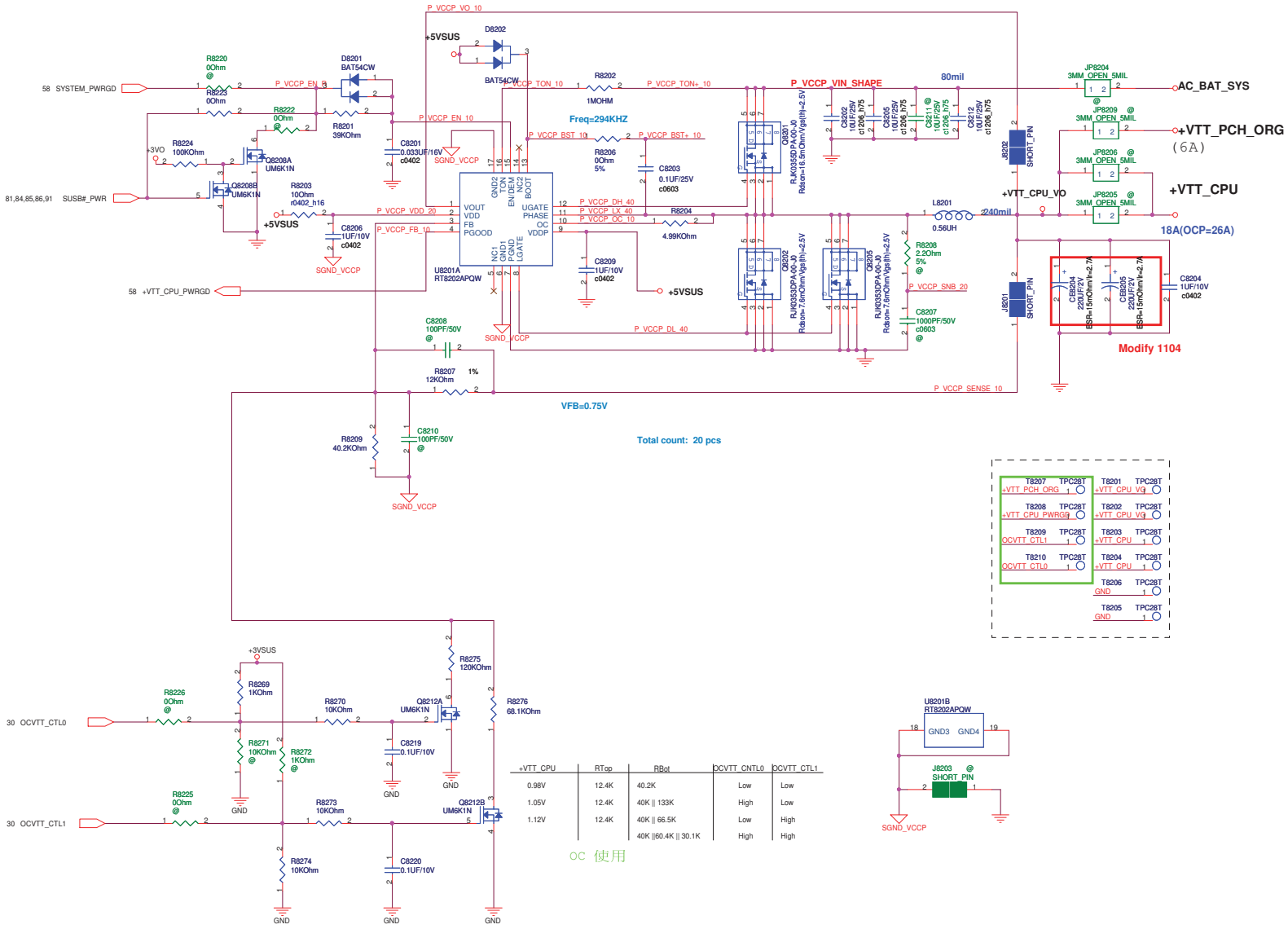
ASUSTeK COMPUTER INC. NB

Engineer: CH

Size	Project Name	Rev
Custom	+3.3VSUS&+5VSUS	1.0

Date: Friday, January 29, 2010 Sheet 81 of 100

+VCCP POWER SUPPLY



+VTT_CPU	RTop	RBot	OCVTT_CNTL0	OCVTT_CTL1
0.98V	12.4K	40.2K	Low	Low
1.05V	12.4K	40K || 133K	High	Low
1.12V	12.4K	40K || 66.5K	Low	High
		40K ||60.4K || 30.1K	High	High

OC 使用

Power stage

+VTT_CPU:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.32A
2. Ripple Current:
   Irip=5.9A
3. Ripple Voltage:
   ESR/1=10mohm
   V=59mV
4. Inductor Spec:
   Isat=30.5A
   Idc=22.9A
   DCR=1.4mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA
   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)
   L-side MOSFET: RJK0353DPA
   Rds(ON)=7.6mohm (Vgs=4.5 V)
   I cont = 35A (T =25 ℃)
   I peak =140 A (Pause =10 us)

Controller

+VTT_CPU

1. Voltage & Current:
   +VCCP: 1.05V / 26A
2. Frequency:
   F=294KHZ
3. OCP:
   Set R8204=4.99 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=26.26A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 220 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.17 A

Part Selection

1. MOSFET:

PPAK56

High Side

RJK0355DPA
07G005B14011(HF)

RJK0355DPA
07G005B14010

Low Side

RJK0353DPA
07G005A92010

PPAK33

High Side

SI7326DN
07G005A80011(HF)

2. Inductor:

Molding063

FDVE0630-H-1R0M=P3
09G02X103506(HF)

PCMC063T-1R0MN
09G02X103022

MPC7301R0M1
09G02X103H11

Ferrite104

FDUE1040D-H-1R0M=P3
09G02X103T25(HF)

PCMC104T-1R0MN
09G02X103U00

MPO104-1R0
09G02X103R01

3. Output Cap:

7343

EEFCX0D221YR
11G08D1227D0

EEFCX0D221R
11G08D2227D1

ACAS2R0S221E15
11G09D2227D0

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_+VCCP

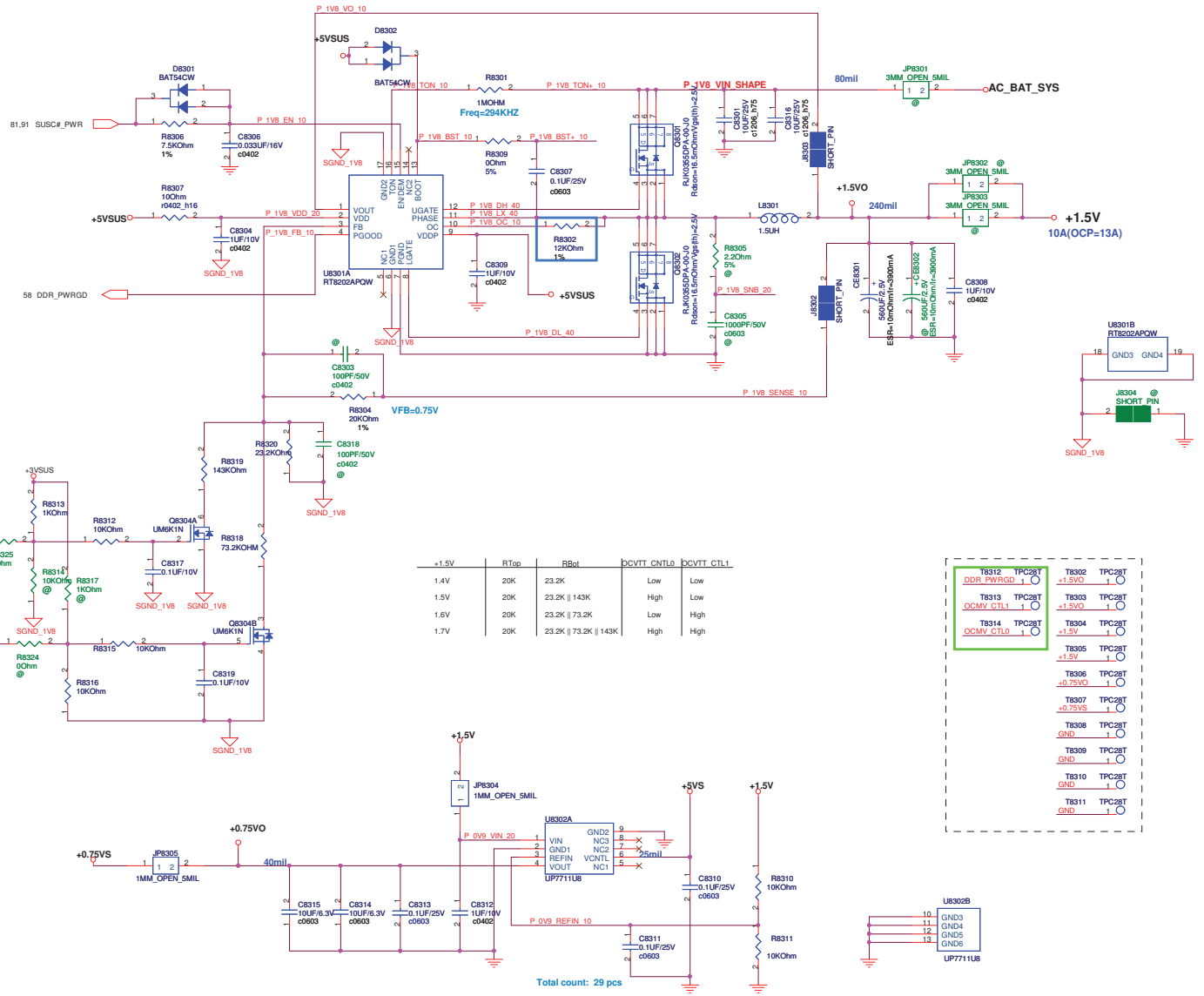
Engineer: CH_LU

Size	Project Name	Rev
C	K72J	1.0

Date: Friday, January 29, 2010 Sheet 82 of 100

http://laptop-motherboard-schematic.blogspot.com/

+1.5V & 0.75VS POWER SUPPLY



+1.5V	RTop	RBot	DCVTT_CNTL0	DCVTT_CTL1
1.4V	20K	23.2K	Low	Low
1.5V	20K	23.2K || 143K	High	Low
1.6V	20K	23.2K || 73.2K	Low	High
1.7V	20K	23.2K || 73.2K || 143K	High	High

Power stage

DDR II:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.052A
2. Ripple Current:
   Irip=3.07A
3. Ripple Voltage:
   ESR/1=10mohm
   V=30.7mV
4. Inductor Spec:
   Isat=10.9A
   Idc=10A
   DCR=12.1mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

Controller

DDR II:

1. Voltage & Current:
   +1.5V: 1.5V / 10A
2. Frequency:
   F=294KHZ
3. OCP:
   Set R8302=12Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=14A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 560 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.17 A

1. Voltage & Current:
   +0.75V: 0.75V / 1A

Part Selection

1. MOSFET:	2. Inductor:	3. Output Cap:
PPAK56	Molding063	7343
High Side	FDVE0630-H-2R2M=P3 09G02X223B09(HF)	EEFCX0D221YR 11G08D1227D0
RJK0355DPA 07G005B14011(HF)	PCMC063T-2R2MN 09G02X223B01	EEFCX0D221R 11G08D2227D1
RJK0355DPA 07G005B14010	MPC730-2R2M01 09G02X223B15	ACAS2R0S221E15 11G09D2227D0
Low Side		
RJK0353DPA 07G005A92010		
PPAK33		
High Side		
SI7326DN 07G005A80011(HF)		

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_DDR

Engineer: CH_LU

Size	Project Name	Rev
Custom	K72J	1.0

Date: Friday, January 29, 2010 Sheet 83 of 100

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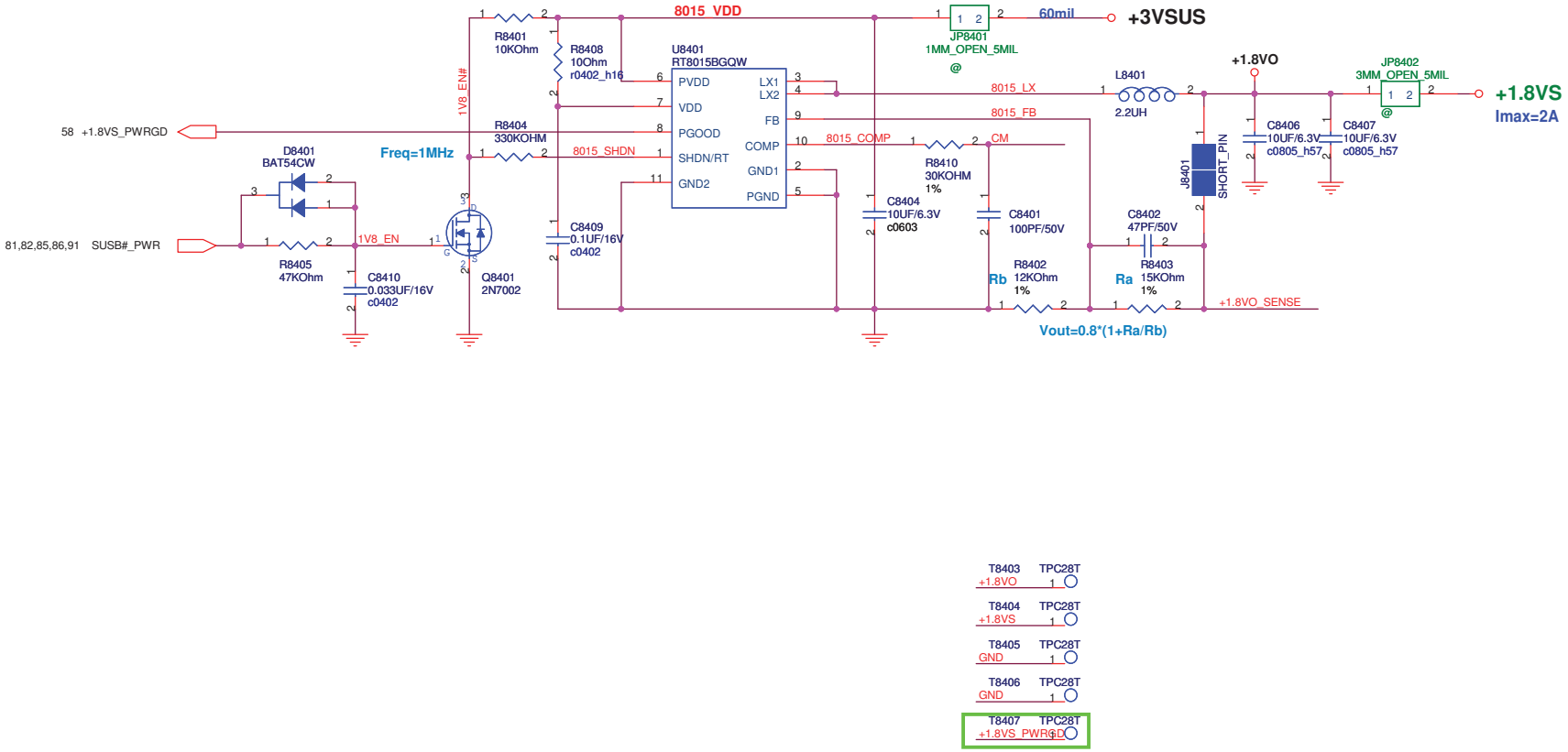
+1.8V POWER SUPPLY



+1.8VS @ 2A

1. Supply Voltage:
   VIN = 3.3V (2.6V ~ 5.5V)
2. Supply Voltage:
   VOUT = 1.8V / 2A
3. Current Limit:
   I limit =3.2A
4. Continue Current:
   I cont = 2A
5. Feedback Voltage:
   VFB = 0.8V
6. Switching Frequency:
   Rrt = 330 Kohm
   Fsw = 1 MHz

T8403	TPC28T	+1.8VO
T8404	TPC28T	+1.8VS
T8405	TPC28T	GND
T8406	TPC28T	GND
T8407	TPC28T	+1.8VS_PWRGD

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_+1.8VS

Engineer: CH_LU

Size	Project Name	Rev
B	K72J	1.0

Date: Friday, January 29, 2010 Sheet 84 of 100

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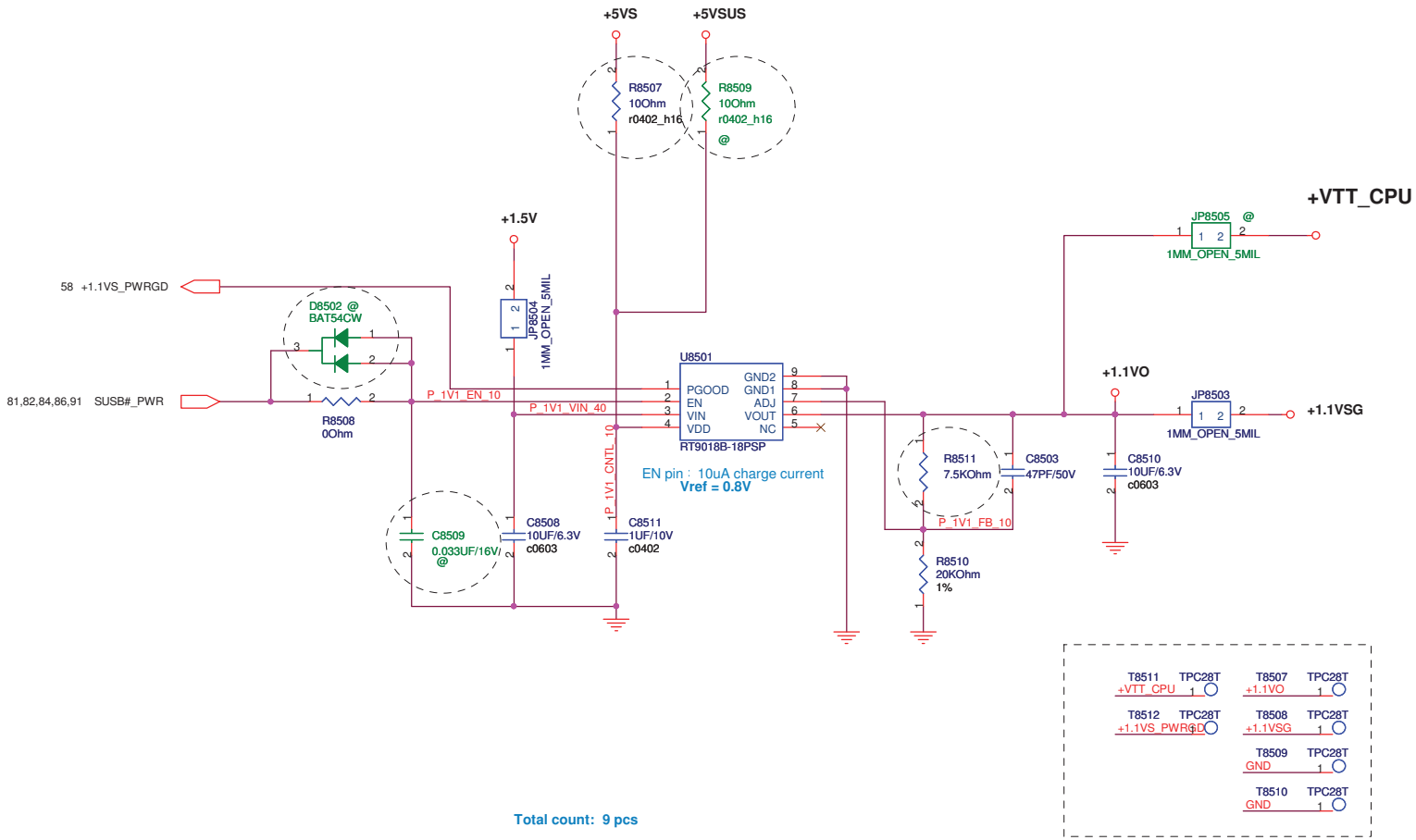

Total count: 9 pcs

+1.1VSG @ 2A

1. Dropout Voltage:

   △V = 0.4V (Io =2A)

2. Current Limit:

   I limit =4A

3. Continue Current:

   I cont = 2A

4. Power Dissipation:

   Rthjc = 52℃/W
   Pd =1.9W

5. EN Voltage:

   V rising = 1.4V
   V falling = 0.8V

6. Supply Voltage:

   VIN =1.5V

7. Inrush current:

   T ss = 5ms
   C total =10uF
   I inrush = 0.003A

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title :

Engineer:

Size	Project Name	Rev
B		1.0

Date: Friday, January 29, 2010 Sheet 85 of 100

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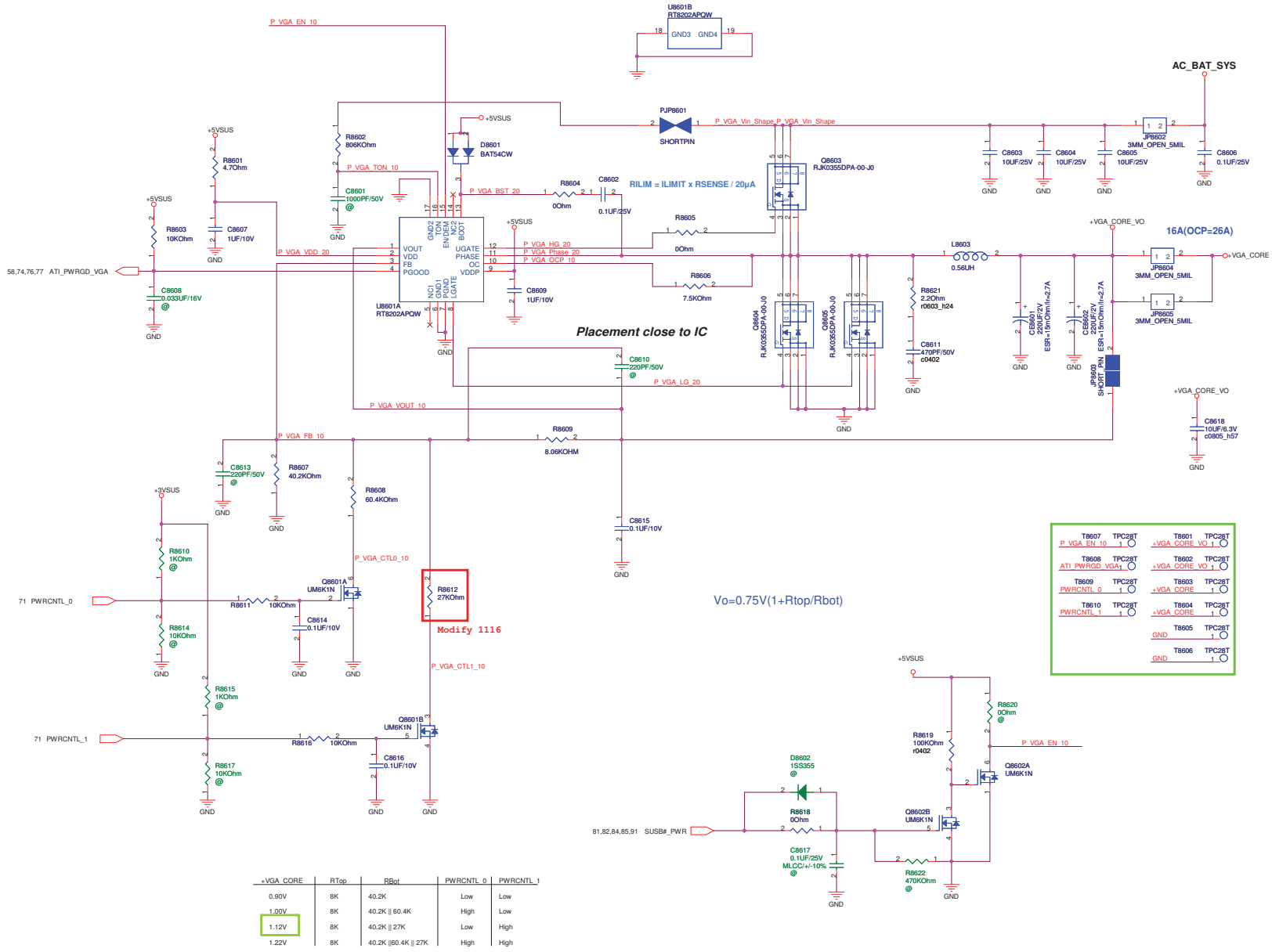

+VGA_CORE	RTop	RBot	PWRCNTL_0	PWRCNTL_1
0.90V	8K	40.2K	Low	Low
1.00V	8K	40.2K || 60.4K	High	Low
1.12V	8K	40.2K || 27K	Low	High
1.22V	8K	40.2K ||60.4K || 27K	High	High

Power stage

+VGA_CORE:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.12A
2. Ripple Current:
   Irip=5.63A
3. Ripple Voltage:
   ESR/2=7.5mohm
   V=42.22mV
4. Inductor Spec:
   Isat=30.5A
   Idc=22.9A
   DCR=1.7mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA
   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)
   L-side MOSFET: RJK0355DPA
   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

Controller

+VGA_CORE:

1. Voltage & Current:
   +VGA_CORE: 1.1V / 16A
2. Frequency:
   F=253KHZ
3. OCP:
   Set R8606=7.5 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=26A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 440 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.296 A

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VGA(RT8202A)

Engineer: CH_LU

Size	Project Name	Rev
Custom	K72J	1.0

Date: Friday, January 29, 2010 Sheet 86 of 100

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<Variant Name>

Title :

<OrgName>

Engineer:

Size	Project Name	Rev
Custom		1.0

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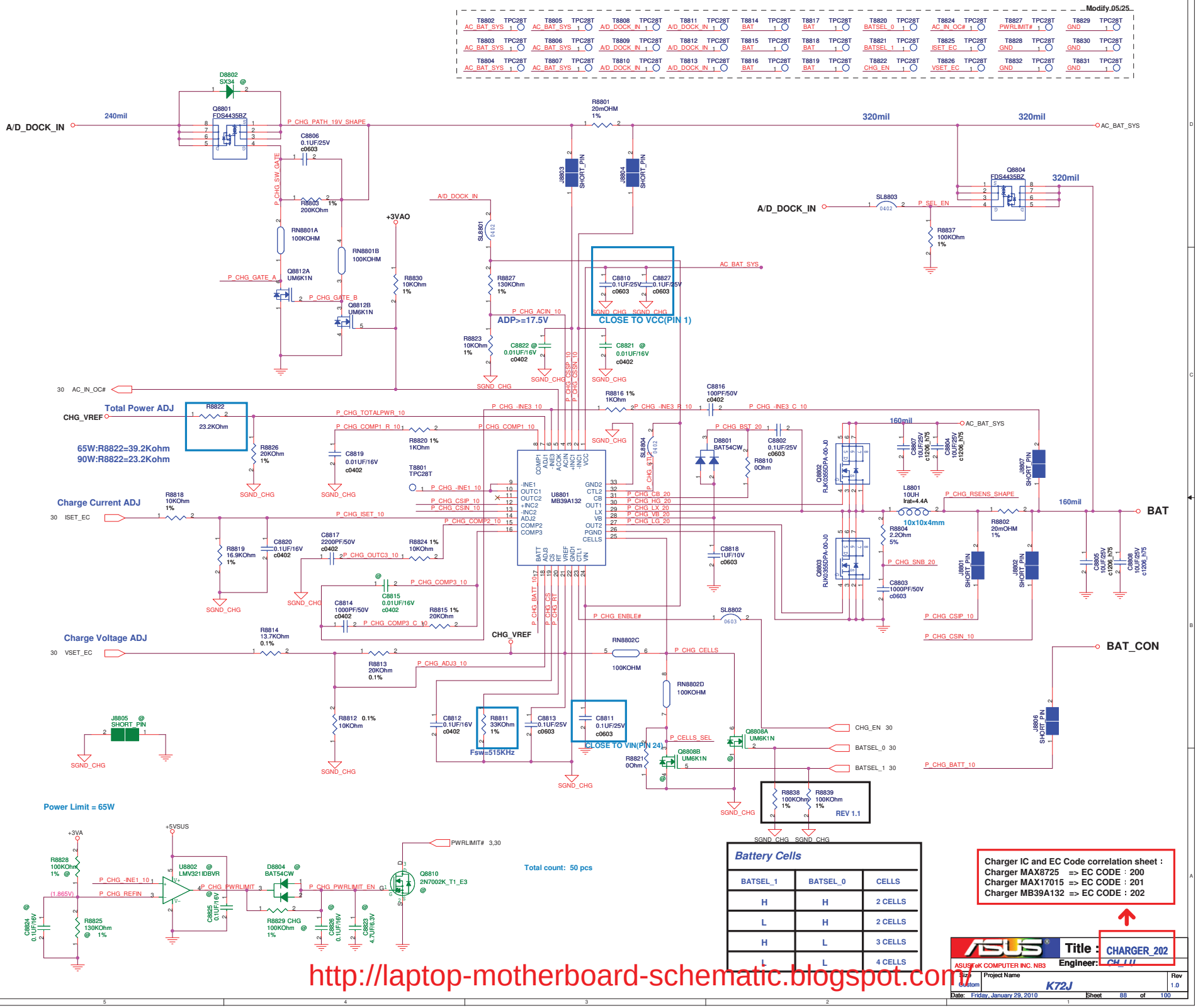

http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

Title :

<OrgName>

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Friday, January 29, 2010 Sheet 89 of 100

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BATTERY IN DETECT

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title :POWER_DETECT	
	Engineer: Morris	
Size: Custom	Project Name: Design IP	Rev: 1.0
Date: Friday, January 29, 2010	Sheet 90 of 100	

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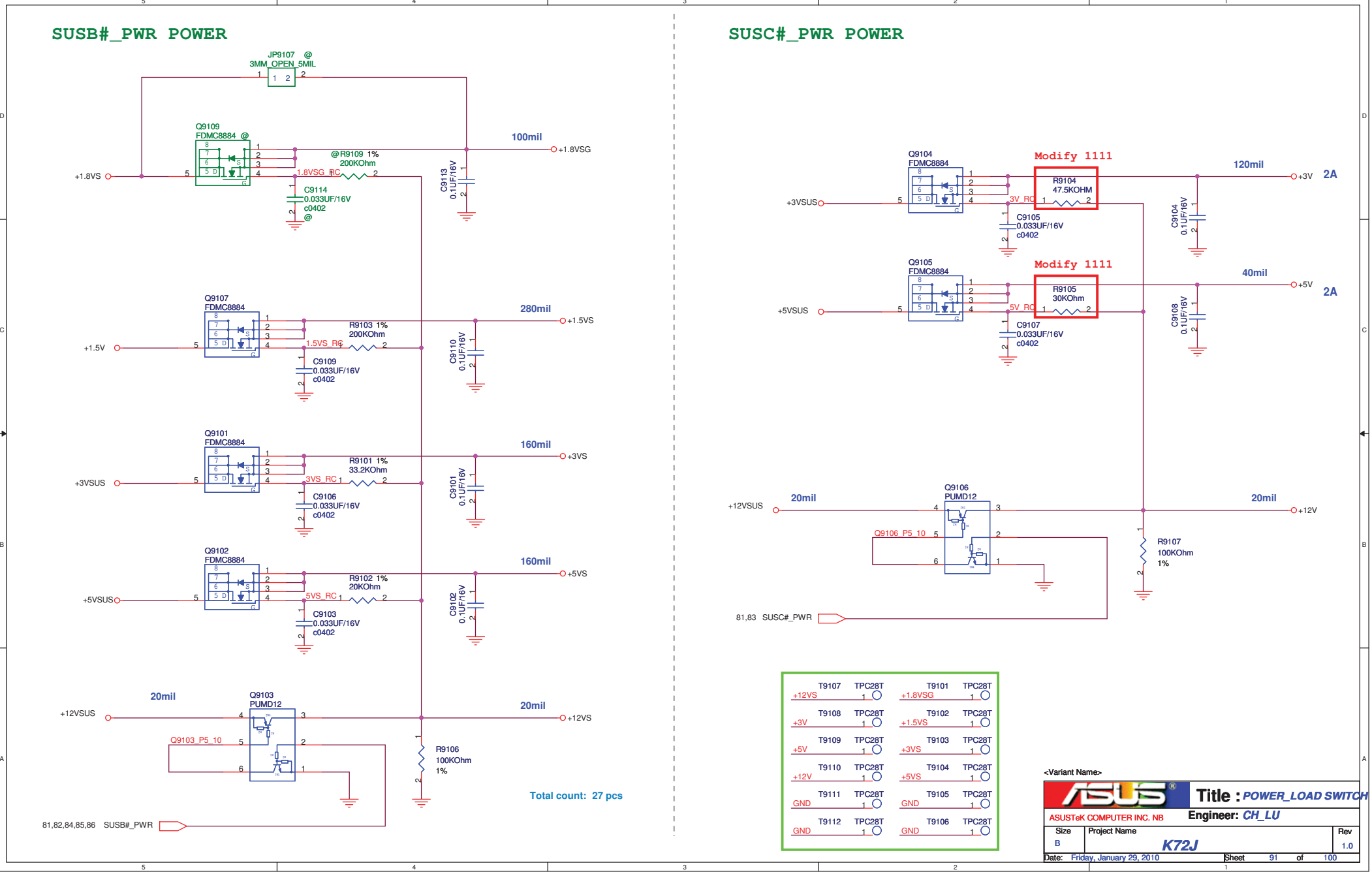

http://laptop-motherboard-schematic.blogspot.com/

History

R1.0 to R1.1 :

Page 3 : Change R0363,R0364 to RN0302.
Remove SL0311,SL0312.
Change R0366,R0367 to SL0319,SL0320.
Change R0351 to SL0321.

Page 5 : DNI R0501,R0502,R0505,R0506.

Page 6 : Remove R0616,R0601.
Change R0607 to SL0601.
Change R0605,R0606 to RN0601.

Page 14 : Change CE1407 from 220uF to 100uF for cost down.
Change CE1401~CE1403,CE1406 from POSCAP to TAN for cost down.
Change JP1402 to R1414,R1415 for EMI request.
Correct CE1404 part reference to C1450.

Page 16 : Change R1605,R1606 to SL1601,SL1602.

Page 17 : Change R1705,R1706 to SL1701,SL1702.

Page 18 : Change C1811,C1802 from 0.1uF/10V to 0.1uF/16V.
Remove R1809,R1810.
Change R1801,R1802,R1803,R1804 to RN1802.

Page 19 : Add OC/UC circuit (IT8268).

Page 21 : Remove RX2105,RX2106,RX2107,RX2108,RX2140,RX2141.
Change R2136,R2137 to RN2101.

Page 22 : Chaneg R2257 to SL2201.
Remove R2245.
Change R2246 to SL2202.
Change R2239,R2240 to SL2203,SL2204.

Page 23 : Change R2322,R2323 to RN2301.

Page 24 : Change RX2401,RX2404,RX2406 from 22ohm to 47ohm.
Remove T2413.
Change RP2401~RP2403 to RN2401~RN2405.
Change Card Reader to USB port 11.

Page 25 : Remove R2504,R2523.

Page 26 : Remove JP2601.
Add D2605,R2623,Q2621,R2637,C2617 for ITE8541.

Page 27 : Change +VTT_PCH to +VTT_PCH_ORG.

Page 28 : Change SPI ROM circuit for ITE8541.

Page 29 : Add R2922 for CLK_PWRGD# (open drain).
Add +VDD_1.05 for ICS9LVS3162.

Page 30 : Add U3004 co-lay with U3003.
Add R3010 for X'tal free option.
Add R3008,R3006 for ITE8541 VSUS_ON.
Add OCVTT_CTL0/1,OCMV_CTL0/1 for OC/UC option.

Page 31 : Change C3105 from 0.1uF/10V to 0.1uF/16V.

Page 33 : Remove R3314.
Remove AR8121 option circuit.

Page 34 : Change Transformer to 09G051059023 / 09G051059055.
Change +AVDD_CEN_LAN to +AVDD_1.7_LAN.

Page 37 : Change Jack Ground from GND_AUDIO to GND_JACK.
Add SL3740 for HP1_JD , SL3741 for EXT_MIC_JD.

Page 45 : Change R4501 from 330ohm to 150ohm.
C4507 from 1uF/10V to 1uF/6.3V.
Change C4511(0.1uF/10V) to C4513(0.1uF/16V).
Change RNX4501,LX4501 to SL4501.
Change C4514 connect to R4529 pin1.
Change L4503,C4509,C4512 connection.

Page 48 : Change VGND to GND.
Change F4801 from 0.2A/30V to 1.5A/6V.
Add D4803.

Page 53 : Remove RX5305,RX5306.

Page 56 : Change C5605 from 0.1uF/10V to 0.1uF/16V.
Change LED5601~LED5603 from BLUE to GREEN.
Change LED voltage from +5VS/+5VA to +3VS/+3VSUS.
Add CAP_LED#,NUM_LED# pull-up for open drain signal.

Page 57 : Change Q5703B to NC , R5708 pin1 to +VTT_CPU_VO.

Page 58 : Add R5836 (DNI).

Page 60 : Remove L6001,L6002.

Page 65 : Add H6502 for LVDS cable.

Page 68 : Add caps for EMI request.

Page 70 : Change VGND to GND.

Page 71 : Remove R7124.

Page 73 : Change VGND to GND.

Page 74 : Change CE7401 from 3528 to 7343 type.
Change all +VGA_CORE 0.01uF to 1uF for PARK.

Page 75 : Add RN7501~RN7507 for dual rank memory.

Page 76 : Change VGND to GND.

Page 80 : Mount R8050,R8052.
Change R8050,R8051,VID pull-up to +VTT_CPU_VO.

Page 82 : Change +VTT_PCH to +VTT_PCH_ORG.
Add OV/UV circuit , remove 1.1V support.

Page 83 : Add OV/UV circuit.

Page 84 : Change R8405 from 330K to 200K ohm for +1.8VS timing.

Page 86 : Change 5V_RUN to +5VSUS , VGND to GND.

Page 91 : Change JP8207 to JP9107.

***** Change all M92 parts to PARK parts *****

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R1.1 to R1.2 :

Page 20 : Change C2001,C2002 from 18pF to 15pF.

Page 24 : DNI U2401 , mount R2413.

Page 26 : DNI D2605 , mount R2623 for ITE8541.

Page 28 : DNI R2848 , mount R2857 for ITE8541.
Mount R2866~R2869 for ITE8541.

Page 29 : DNI L2904 & R2921 , mount L2903 for ICS9LVS3162.

Page 30 : DNI R3008 , mount R3006 for ITE8541.
Change C3016,C3017 from 15pF to 10pF.
DNI U3003,R3014 , mount R3002~R3005 for ITE8541.

Page 33 : Add R3321 for signal integrity.

Page 36 : Add D3601 for pop noise.

Page 37 : Change D3709 from RB717F to BAT54AW.
Change C3701 to X7R.

Page 45 : Change C4504 from 1uF/10V to 1uF/6.3V.

Page 47 : Change C4804~C4811 to X5R type.
Change R4801,R4802 to RN4801.

Page 57 : DNI R5705,R5706,Q5703,R5708,R5714,R5715,Q5707,R5712.

Page 58 : Change D5801 from BAT54CW to BAT54C.

Page 65 : Remove H6521,H6522,H6506,H6507,H6523,H6524.

Page 74 : Change L7405 to 09G013120400.
DNI Q7401,L7407 , mount R7402.
Change R7402 to 0805 type.

Page 75 : DNI R7501 for PARK.
Change pin AL21 to test point.

Page 82 : DNI R8220 & R8222 , mount R8223.
Add R8225 & R8226.
DNI R8271 & R8272.

Page 83 : Add R8324 & R8325.
DNI R8314 & R8317.

Page 84 : Change R8405 from 200K to 47K ohm for +1.8VS timing.

Page 85 : Add JP8505 , R8509.
Change R8511 from 7.5K to 5.1K ohm.
DNI U8501 related circuit for cost down.

R1.2 to R1.3 :

Page 21 : Change R2157 from 39 ohm to 15 ohm for single load.

Page 25 : Change PCB ID resistors.

Page 30 : Change R3021,R3023 from 47K ohm to 100K ohm for battery team request.
Add R3030 for VSUS_ON connection.
Delete J3001 & U3004 from schematic.
Add R3011 & Q3002 for ITE8570 X'tal free option.

Page 38 : Change R3852 to 0 ohm , C3801 to DNI.

Page 40 : Change SL4501 to L4502 for EMI request.

Page 52 : Change SL5201,SL5202 to L5201,L5202 for EMI request.

Page 65 : Modify H6518 shape for ME request.

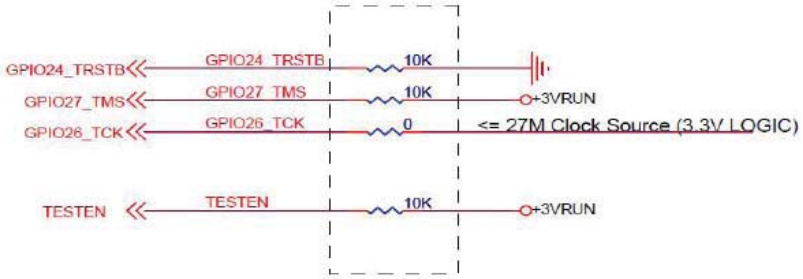
Page 71 : Change R7128 to 0402 type.

Page 77 : Change R7714 to /HYNIX , R7718 to /SAMSUNG.

Page 80 : Change 8029 to 5.36K , C8001 to 68nF , R8032 to 10K , C8019 to 220pF.
Change R8039,R8040 to 165K ohm.

Page 82 : Change CE8202 to C8221 & C8222 (DNI).

Page 70~77 : Add PARK errarta items as below.



In current reference design, TESTEN is pulled down through a resistor and GPIO24_TRSTB may be pulled-high or floating. To implement option 2, both of these resistors should be depopulated (keep the resistor pad for debugging purposes).

Option 2 requires that:

1) TESTEN and GPIO27_TMS be pulled high (3.3V)

2) GPIO24_TRSTB be pulled to ground (0V), and

3) A clock source (1KHz -27MHz, 3.3V level) be provided on GPIO26_TCK (through a 0 Ohm resistor). The 27MHz oscillator output can be used (if present).

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R1.3 to R2.0 :

Page 19 : Add R1903.

Page 20 : DNI R2034~R2039 for Production PCH.

Page 21 : Change R2157 from 15 ohm to 24.9 ohm.

Page 32 : Mount R3207 for G709.

Page 36 : Change INT_MIC to Codec Port A for feedback issue.

Page 37 : Change Phone Jack P/N from 12G14030106L to 12G14000106M.

Page 38 : Change Internal Mic reference voltage to codec output.

Page 46 : DNI Q4601 , mount U4601 , change SL4601 & SL4602 to 33 ohm for HDMI audio disappear issue.

Page 48 : DNI D4803 for cost down.

Page 50 : Add G709 circuit , DNI G781 circuit.

Page 51 : Change R5101~R5103 to short land.

Page 56 : Change LED5601 from Green to White , R5604 pin1 from +3VSUS to +5VSUS.

Page 57 : Delete Q5702 & Q5703 & Q5707 discharge circuit , change Q5704 to 2N7002.

Page 60 : Delete JP6003 & JP6004.

Page 65 : Delete H6527.

Page 66 : Change C6607 from 0.1uF/16V to 0.1uF/25V.

Page 71 : Add U7101 & R7131 for PARK errata E2 , DNI R7121 & R7124 for production PARK.

Page 73 : DNI R7335 , mount R7305 for production PARK.

Page 76 : DNI R7605 for production PARK.

Page 82 : Modify CE8204 & CE8205 package.

Page 91 : Change R9104 to 47.5K , R9105 to 30K for power on fail issue.

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